ECE 409 - ERROR CORRECTING CODES - INVESTIGATION 25
INTRODUCTION TO CONVOLUTION CODES - PART II

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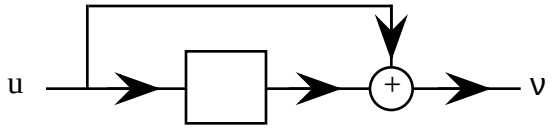
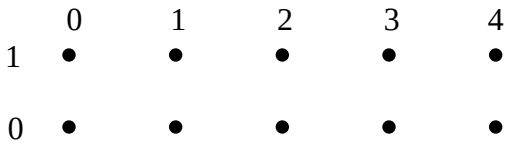
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

From the last Investigation we know how to build convolution encoders. The objective of this Investigation is to introduce the use of trellises for the decoding of convolution codes.

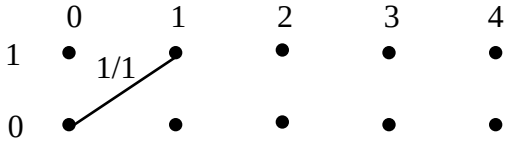
1. The objective of this and the next several problems is to introduce trellises. Let us begin with the following simple encoder



The trellis for such a circuit is a diagram as follows



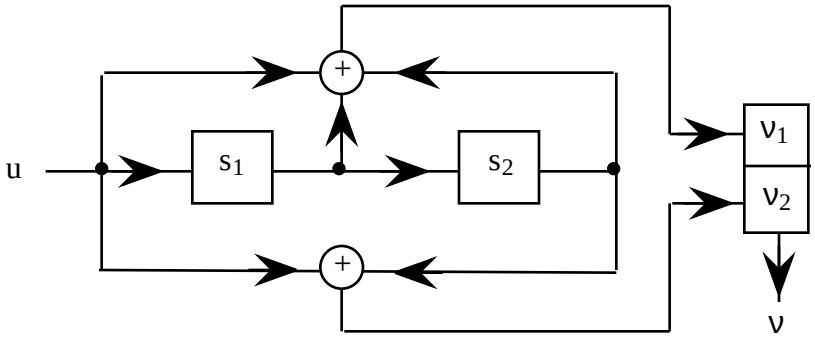
that traces the state of the encoder - the value of its flip-flops - as input bits are entered. The rows of the trellis are the states while the columns are for the clock pulses clocking the data bits into the circuit. Note that we always assume that the encoder starts off in the zero state. Suppose in particular that the first input bit to the encoder is a 1. Then we show this on the trellis with a line as follows



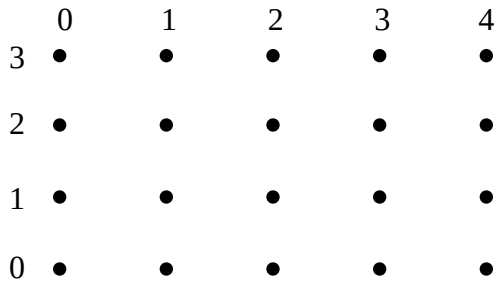
that goes from the present to the next state. Note that the 1 on the line is equal to the output when the encoder is in state 0 and the input is 1.

   a. Find and draw the state diagram or next state table for the circuit
   b. Make use of your state diagram or state table in part (a) to draw the path through the trellis when the input is u=100110. Assume as before that the first bit entered into the encoder is the bit on the left. Use a solid line when the input is a 1 and a dashed line when the input is a 0

2. Given the following convolution encoder

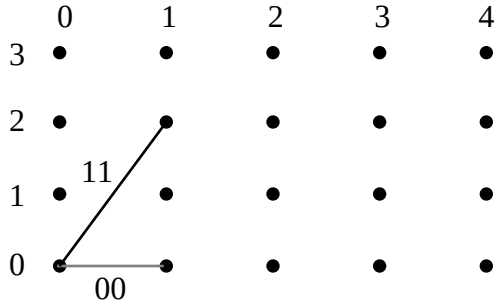


with two outputs $\nu_1\nu_2$ and four states s_1s_2 and so a trellis that looks as follows



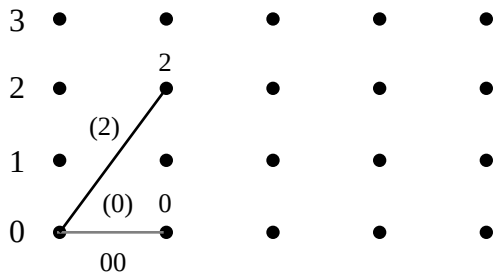
a. Draw the state diagram or next state table for the circuit
b. Trace the path through the trellis for the input u=100100. Assume that the first bit entered is the one on the left. Make sure your result ends up back at the zero state
c. Draw all paths that start in the zero state and end in the zero state after 4 clock pulses

3. Complete the following trellis showing every possible path for the convolution circuit in Problem (2) up through 4 clock pulses. Draw solid lines for when the input is equal to 1 and dashed lines for when it's equal to 0 as follows



Alongside the lines we have written the corresponding output of the encoder

4. A trellis can be used to decode a received signal with errors - to find the code that was most likely to have been sent - by tracing paths through the trellis as follows



From every reachable state we draw lines to the next possible states - the state that the encoder would go to if the input was a 0 and the state it would go to if the input was a 1. The 2-bit number at the bottom is the input to the decoder - the received signal. The numbers in parenthesis above the lines are the number of errors in the received signal that would have had to occur if this was the real path. The numbers above the dots are the total number of errors along the path from the origin.

Since the input in this case is 00 we have errors of 0 and 2 as shown. If two paths both go to the same dot - the same state - then we choose the one with the smallest error and put an x through the last line of the other path leading to the dot. This scheme is referred to as the **Viterbi algorithm**.

Given the following received signal

$$w = (11\ \ 10\ \ 01\ \ 10\ \ 11\ \ 00)$$

originally generated by the circuit in Problem (2)

a. Draw the corresponding trellis to find the path with least error
b. Identify the path with least error and the corresponding values of the data