ECE 207L - FIRST ORDER RC CIRCUITS - LAB 17
FANOUT IN CMOS INTEGRATED CIRCUITS

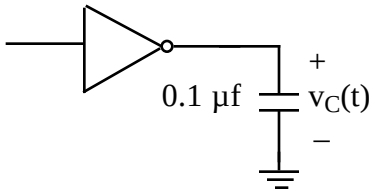
FALL 2003 **A.P. FELZER**

OBJECTIVE

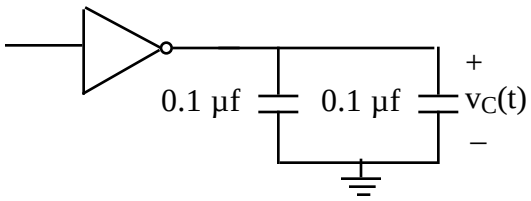
The objective of this lab is to model the affects of fanout in CMOS integrated circuits.

LAB

1. Given the following circuit with the capacitor modeling the input capacitance of a CMOS gate connected at the output of the inverter



   a. Measure your capacitor value and then compare it with its nominal value
   b. Measure the time it takes $v_C(t)$ to increase from 0 volts to 4 volts during pull-up and the time it takes $v_C(t)$ to decrease from 5 volts to 1 volt during pull-down
   c. Now add a second capacitor to modeling the connection of a second gate to the output as follows



      and again measure the time it takes $v_C(t)$ to increase from 0 volts to 4 volts during pull-up and the time it takes $v_C(t)$ to decrease from 5 volts to 1 volt during pull-down
   d. What's the relationship between the pull-up times you measured in parts (b) and (c) and what's the relationship between the pull-down times you measured in parts (b) and (c)
   e. Explain the relationships you described in part (d)