# ECE 207L - FIRST ORDER RC CIRCUITS - LAB 16
# INTERCONNECTS IN CMOS INTEGRATED CIRCUITS

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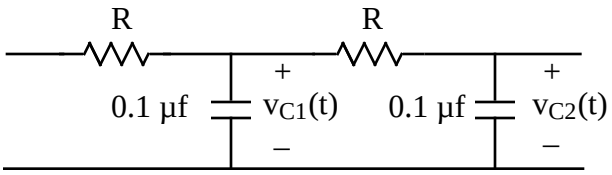
## OBJECTIVE

The objective of this lab is to model the affects of the interconnects in CMOS integrated circuits with two lump RC circuits.

## LAB

1. Given the following two lump RC circuit for modeling interconnects in CMOS integrated circuits




PARTNER 1: R = 1K PARTNER 2: R = 2K

a. Measure your resistor and capacitor values. Compare with nominal values
b. Sketch what you expect for $v_{C2}(t)$ during pull-up assuming the voltages across the capacitors start from 0 volts. What is the final steady state value
c. Sketch what you expect for $v_{C2}(t)$ during pull-down assuming the voltages across the capacitors are initially 5 volts
d. Now connect up your circuit to the scope and make use of what you see to sketch $v_{C2}(t)$ during pull-up and during pull-down. How do your sketches compare to what you expected in parts (b) and (c)
e. Measure the time it takes $v_{C2}(t)$ to increase from 0 volts to 4 volts during pull-up and the time it takes $v_{C2}(t)$ to decrease from 5 volts to 1 volt during pull-down
f. Do the analysis to come up with equations for $v_{C2}(t)$ during pull-up and pull-down.
g. Make use of Mathcad to plot your equations in part (f)
h. Make use of your graphs in part (g) to find the time it takes $v_{C2}(t)$ to increase from 0 volts to 4 volts during pull-up and the time it takes $v_{C2}(t)$ to decrease from 5 volts to 1 volt during pull-down
i. Compare your calculated and measured results in parts (e) and (h)