ECE 207L - FIRST ORDER RC CIRCUITS - LAB 13
TIME DELAY OF LOGIC INVERTERS

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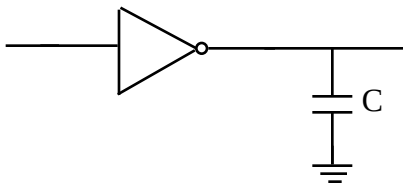
OBJECTIVE

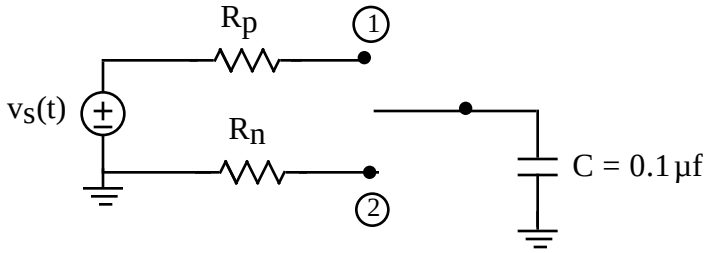
The objective of this lab is to illustrate how the pull-up and pull-down resistors R_n and R_p of a CMOS gate can be approximated.

LAB

1. If we connect a known capaictor C to a CMOS inverter as follows



with equivalent circuit as follows



then we should be able to calculate R_n and R_p by measuring the time constants τ_{pu} and τ_{pd} for pull-up and pull-down when the input $v_s(t)$ is a pulse train. Do this for your inverter as if it was a CMOS inverter. Note that you'll have to keep increasing the frequency of the input pulse train until you get a good display of the transient response