ECE 207 – FIRST ORDER RC CIRCUITS – INVESTIGATION 17
FANOUT IN CMOS INTEGRATED CIRCUITS

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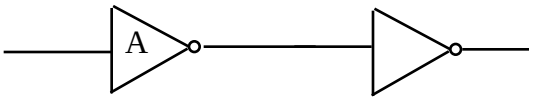
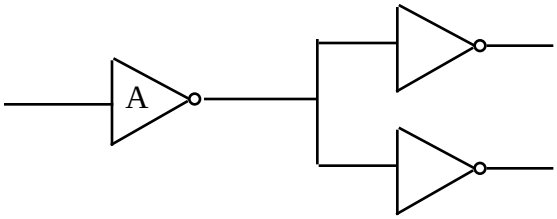
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

The objective of this investigation is to calculate what happens when more than one inverter is connected to the output of a logic gate in a CMOS integrated circuit.

1. Up to now we've only been analyzing logic circuits like the following



with Inverter A *driving* only one other inverter. The objective of this problem is to analyze a circuit with Inverter A driving two inverters as follows

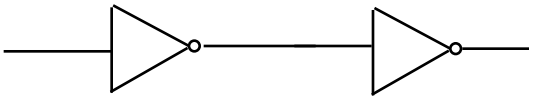


Note that the **fanout** of a logic gate is the most gates it can drive and still meet its specs.

Given that the inverters in the circuit above has the parameters R_n = 1K, C_n = 5 fF, R_p = 1.5K and C_p = 10 fF

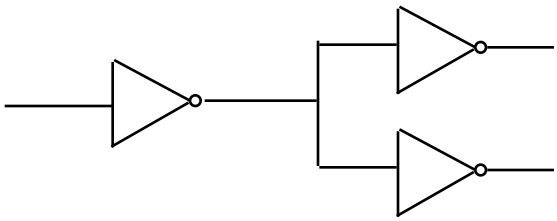
   a. Draw the equivalent circuit - ignore the interconnect
   b. Combine series and parallel resistors and capacitors
   c. Find the pull-up and pull-down times if v_{tl} = 1 volt and v_{th} = 4 volts
   d. What's the fastest clock rate for this circuit - ignoring the interconnect

2. Given that the pull-up and pull-down time constants of the following logic circuit



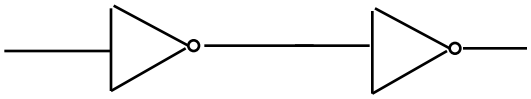
are τ_u and τ_d

   a. What are the pull-up and pull-down time constants of the following circuit



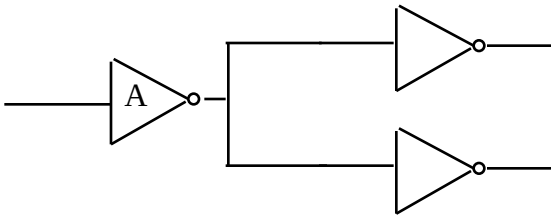
How do you know.

b. What are the pull-up and pull-down time constants when the first inverter is driving n inverters
c. How does an increase by a factor of n in the time constants like in part (b) affect the pull-up and pull-down times - and as a result the maximum clock rate of the circuit
d. What is the maximum clockrate of an inverter driving three other inverters if the maximum clock rate of the following circuit



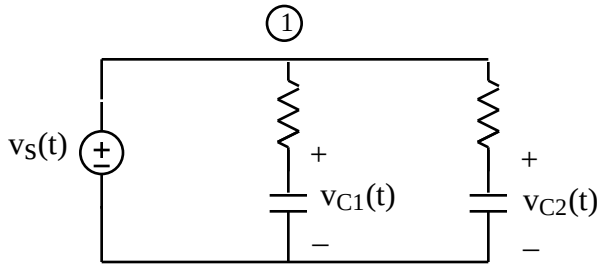
is 100MHz.

3. The objective of this problem is to set up the equations for analyzing a logic circuit with A driving two inverters as follows



when we include the affects of the "long wires" connecting the inverters. Given that R_n = 1K, C_n = 5 fF, R_p = 1.5K and C_p = 10 fF and R_i = 1K, C_i = 2fF

a. Draw the equivalent circuit for the one-lump model
b. Combine series and parallel resistors and capacitors in your circuit in part (a)
c. Write the coupled first order linear differential equations for v_{C1} and v_{C2} during pull-up where v_{C1} and v_{C2} are the voltages across the equivalent capacitances of the circuit. Hint - First write the node equation at node 1 of your equivalent circuit as follows



and find v_1 in terms of v_{C1}, v_{C2} and v_S. Then make use of your result to express i_{C1} and i_{C2} in terms of v_{C1}, v_{C2} and v_S.

d. Make use of your results in part (c) to find the natural frequencies and form of the natural response of the circuit