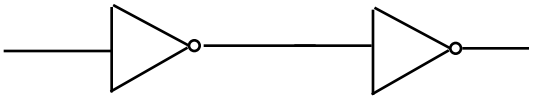
ECE 207 – FIRST ORDER RC CIRCUITS – INVESTIGATION 16
INTERCONNECTS IN CMOS INTEGRATED CIRCUITS

FALL 2000 **A.P. FELZER**

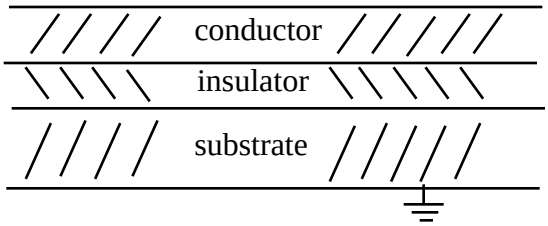
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

The objective of this investigation is to model and calculate the affects of the **interconnects** in CMOS integrated circuits - the conductors that connect the logic gates.

1. When we look at a side view of the interconnect between two logic inverters in a CMOS integrated circuit as follows

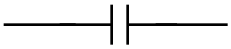


we see a conductor on top of an insulator which is on top of the substrate as follows



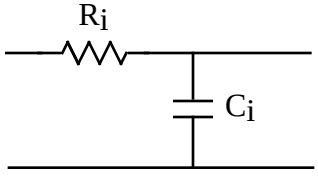
And so the interconnect is not just a conductor which could be modelled by a nice simple resistor as follows

but also a capacitor as formed by the conductor, insulator and substrate. Our problem in modeling such a circuit is that the capacitance is *distributed* all along the length of the conductor - it is not one single **lumped** capacitor as follows



What we have is a **distributed RC circuit** with a symbol as follows

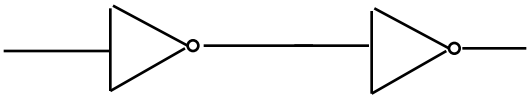
But not all is lost. We can still approximate distributed RC circuits with lumped R's and C's. The simplest model for such an interconnect is the **one lump model** consisting of one resistor together with one capacitor as follows



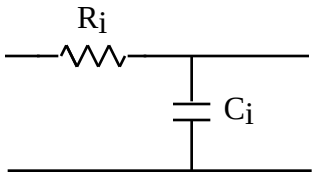
where R_i is the resistance of the conductor alone and C_i the capacitance of the capacitor alone. This model is not perfect but at least it gives a reasonable ballpark approximation of what's

going on during pull-up and pull-down.

a. Draw the equivalent circuit at the interface between these two CMOS inverters



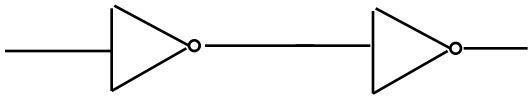
if R_n = 1K, C_n = 5 fF, R_p = 1.5K and C_p = 10 fF and the interconnect is modeled by the following one lump approximation



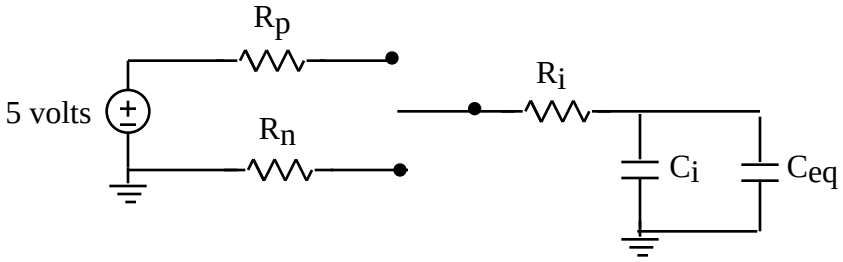
with R_i = 1K and C_i = 10 fF

b. Combine the series and parallel R's and C's in your model in part (a)
c. Calculate the pull-up and pull-down times for your circuit in part (b) if v_{tl} = 1 volt and v_{th} = 4 volts.
d. By how much does the interconnect affect the pull-up and pull-down times.

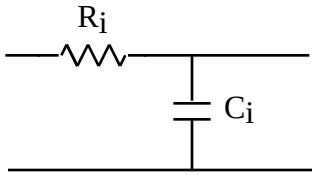
2. From Problem (1) we know that we can approximate the interface between two CMOS inverters as follows



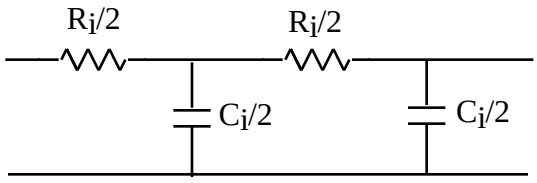
with a one-lump model as follows



The objective of this problem is to approximate the interconnects by two lump models. What we do is simply take our one lump approximations as follows

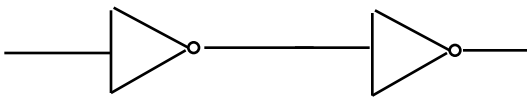


and "divide it into two pieces" as follows



to more resemble a distributed RC circuit.

a. Draw the equivalent circuit for the interface between the following two CMOS gates



if R_n = 1K, C_n = 5 fF, R_p = 1.5K and C_p = 10 fF and for the interconnect R_i = 1K and C_i = 10 fF

b. Combine the series and parallel R's and C's in your circuit in part (a)
c. Write the node equations for your circuit in part (b)
d. Equations like those from part (c) are referred to as **first order coupled linear differential equations**. Put yours in matrix form as follows

$$\begin{pmatrix} v_1' \\ v_2' \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} + \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} (v_s)$$

3. The objective of this problem is to show how coupled first order linear differential equations like those in Problem (2) can be solved. Generalizing on the results of first order linear differential equations, it can be shown that the natural frequencies of coupled differential equations as follows

$$\begin{pmatrix} v_1' \\ v_2' \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} + \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} (v_s)$$

are the roots s_1 and s_2 of the determinant of

$$\left| \begin{pmatrix} s & 0 \\ 0 & s \end{pmatrix} - \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \right| = \begin{vmatrix} s - a_{11} & -a_{12} \\ -a_{21} & s - a_{22} \end{vmatrix}$$

a. Find the natural frequencies of the coupled first order linear differential equations

$$\begin{pmatrix} v_1' \\ v_2' \end{pmatrix} = \begin{pmatrix} -0.75 & 0.25 \\ 0.5 & -0.5 \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} + \begin{pmatrix} 0.5 \\ 0 \end{pmatrix} (5)$$

b. Find the forced responses of $v_1(t)$ and $v_2(t)$ in part (a). Hint - use the same procedure as for first order differential equals. Substitute in $v_1(t) = A_1$ and $v_2(t) = A_2$ and then solve for A_1 and A_2
c. When the natural frequencies are **real and different** as they are in part (a) - and always are in RC circuits - then the natural responses of $v_1(t)$ and $v_2(t)$ are of the following form

$$v_n(t) = K_1 e^{s_1 t} + K_2 e^{s_2 t}$$

where K_1 and K_2 depend on the initial condition of the **complete** response. Find and sketch the complete response of $v_1(t) = v_n(t) + v_f(t)$ in part (a) assuming that $v_1(0) = v_2(0) = 0$. Hint - first make use of the equations in part (a) to find $v_1'(0)$ and then make use of $v_1(0)$ and $v_1'(0)$ to find K_1 and K_2 in the complete response

$$v_1(t) = K_1 e^{s_1 t} + K_2 e^{s_2 t} + A_1$$

where A_1 is the forced response of $v_1(t)$ from part (b).

4. How long will it take the following response to reach steady state - for the natural response to decay to zero

$$v(t) = -3e^{-1000t} - 2e^{-5000t} + 5$$

Explain in words why we can ignore the term $2e^{-5000t}$