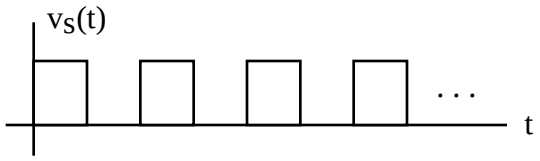
ECE 207 – FIRST ORDER RC CIRCUITS – INVESTIGATION 15
PULSE TRAIN RESPONSES

FALL 2000 **A.P. FELZER**

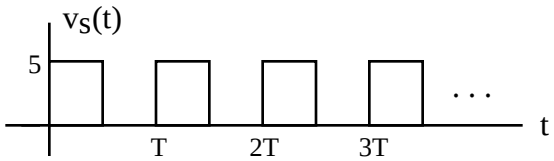
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

From the last investigation we know how to find the pulse responses of first order RC circuits. The objective of this investigation is to see how such circuits respond to pulse trains - periodic signals of pulses (for $t > 0$) as follows



Pulse trains are of particular interest since they are what we see in digital circuits all the time.

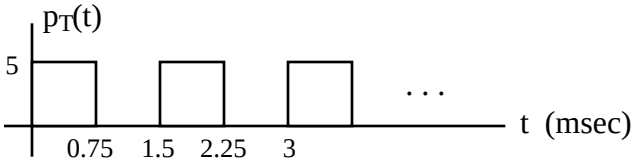
1. We say that the following pulse train



is periodic (for $t > 0$) with period T because it satisfies

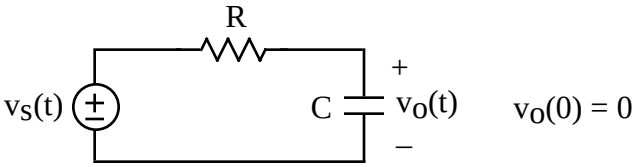
$$v_S(t) = v_S(t + T)$$

   a. Describe in your own words what it means for a signal to be periodic of period T
   b. Verify that $v_S(t) = v_S(t + T)$ for the above pulse train at $t = 0.5$ msec and at $t = 1.2$ msec if $T = 2$ msec. Put your results in a Table.
   c. What is the period of the following pulse train



   d. Draw a pulse train of period $T = 5$ msec

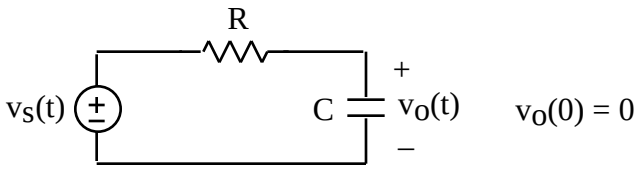
2. Given the following circuit



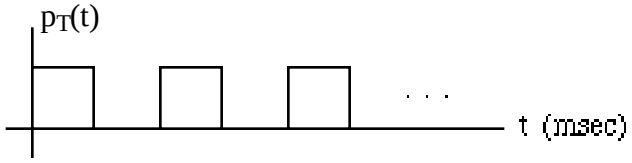
with $v_S(t)$ equal to a pulse train of period T

a. Sketch the first couple of cycles of $v_O(t)$ if $T = 10\tau$
b. Describe what's going on in the circuit as the pulse train turns ON and OFF

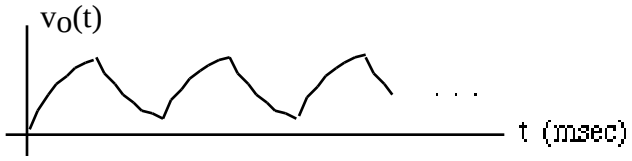
3. The objective of this and the next problem is to review two important results of linear differential equations that are helpful in analyzing linear circuits with periodic inputs. The first result is that the respone of a linear circuit like the following first order RC circuit



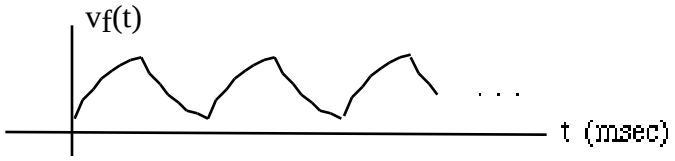
to a pulse train as follows



will be a signal as follows



that is the sum of a natural response $v_n(t)$ plus a forced response $v_f(t)$ just like when the input is a constant. The only difference is that now the forced response will be a periodic rather than constant signal as follows



a. Sketch the natural response for the RC circuit above. How long will it take this natural response (transient response) to decay and the circuit reach steady state if $\tau = 2$ msec
b. Sketch the forced response to the pulse train. Note that we refer to the forced response of a linear circuit to a periodic signal as its **steady state response** since it goes on "forever" once the natural response has decayed. Make sure that your responses $v_n(t)$ and $v_f(t)$ add up to $v_O(t)$

4. The objective of this problem is to demonstrate the fact that the forced responses of linear differential equations satisfy superposition. In particular, show that for the following first order linear differential equation

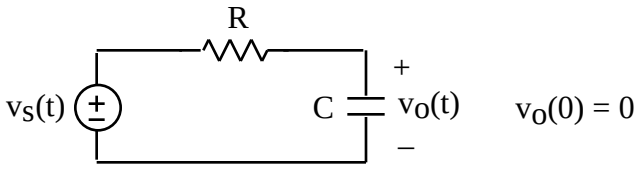
$$x' + 100x = f(t)$$

that if $x_{f1}(t)$ is the forced response when $f(t) = f_1(t)$ and $x_{f2}(t)$ is the forced response when $f(t) = f_2(t)$ for arbitrary functions $f_1(t)$ and $f_2(t)$ like sinusoids, pulses, pulse trains and so on. Then the forced response to $f_1(t) + f_2(t)$ satisfying

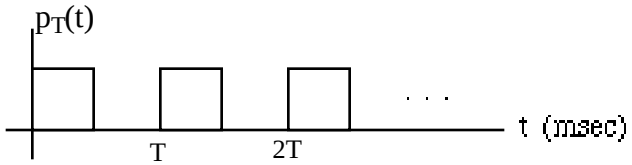
$$x' + 100x = f_1(t) + f_2(t)$$

is $x_f(t) = x_{f1}(t) + x_{f2}(t)$. Do this by substituting $x_f(t)$ into the left hand side of the differential equation and showing that it equals $f_1(t) + f_2(t)$. **Memorize** this result forever.

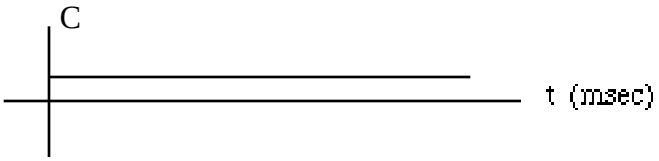
5. The objective of this problem is to sketch the response of the following first order RC circuit



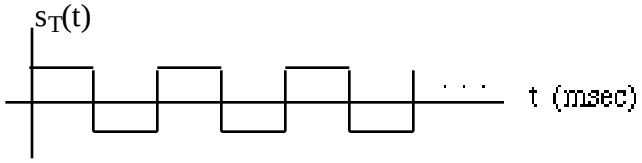
to the pulse train



equal to the sum of the following constant



and squarewave



a. Sketch the forced response to the constant
b. Sketch the forced response to the squarewave if $T = 4\tau$
c. Now make use of the superposition of forced responses to sketch the response to the pulse train.
d. How would a decrease in τ affect the forced response

6. Of particular interest in digital circuits is how fast the frequency of the pulse train can be and the logic gate still have time to make it up to v_{th} and down to v_{tl} during each cycle. This is often done by first calculating the time τ_{pu} it takes the gate to pull-up from 0 volts to v_{th} volts and then time τ_{pd} it takes the gate to pull-down from 5 volts to v_{tl} volts and see which takes longer. The maxium frequency is then the *smaller* of

$$f = \frac{1}{2t_{pu}} \quad \text{and} \quad f = \frac{1}{2t_{pd}}$$

a. What's the highest frequency a CMOS inverter can operate if R_n = 1K, C_n = 5 fF, R_p = 1.5K and C_p = 10 fF if v_{tl} = 1 volt and v_{th} = 4 volts
b. Would you buy CMOS inverters with large or small R's and C's. Why