ECE 207 – FIRST ORDER RC CIRCUITS – INVESTIGATION 12
BASICS OF CMOS GATES

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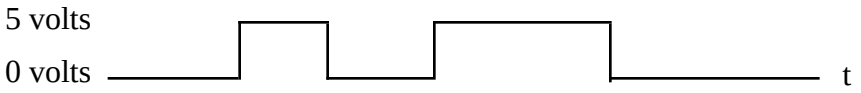
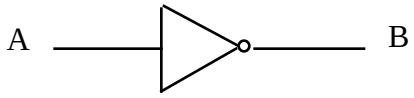
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

In earlier investigations we showed how controlled sources can be used in the modelling of linear amplifiers made from op amps. The objective of this and the next several investigations is to show how capacitors are used in the modelling of digital circuits - circuits we refer to as **logic gates**.

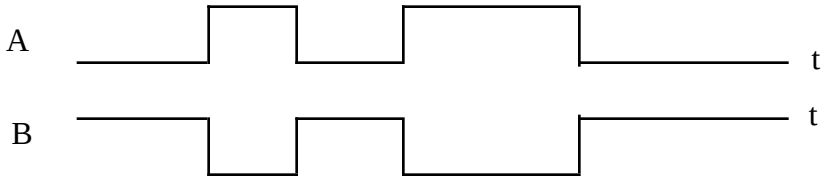
Logic gates are characterized by the fact that their inputs and outputs look as follows



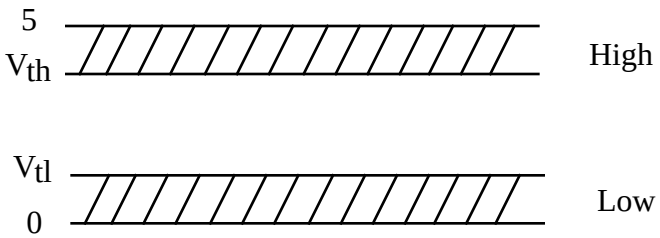
At any give time, these signals are either at their low values, their high values or in transition between the two. Our goal is to estimate how fast digital circuits can operate - how fast they can switch back and forth between these values. We will be focusing on **logic inverters** as follows



with timing diagrams that look - at least ideally - as follows



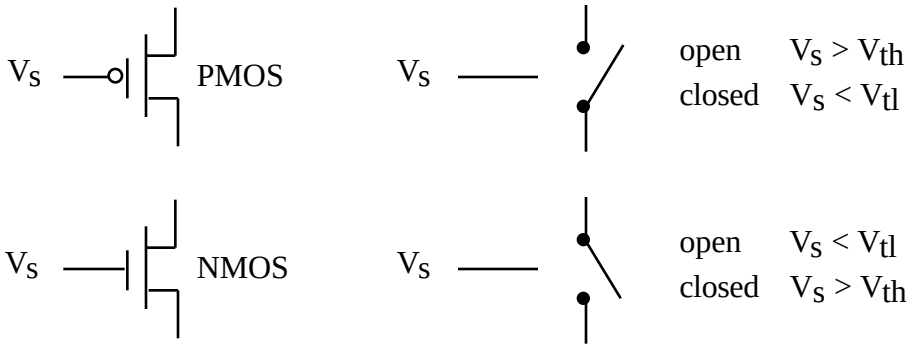
We call such circuits inverters because at any given time the value of the output B is equal to the "opposite" of the input A. When A is high then B is low and when A is low then B is high. As a practical matter we say that a signal V is low when it's in the range $0 \le V \le V_{tl}$ and high when it's in the range $V_{th} \le V \le 5$ as indicated in the following diagram



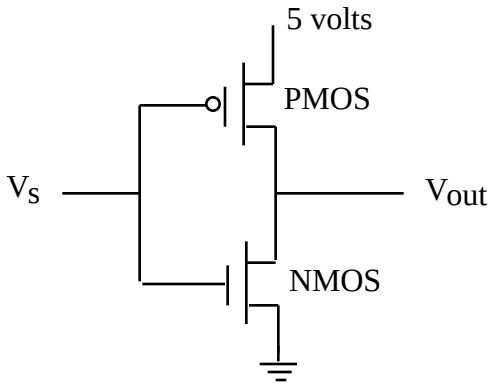
where V_{tl} and V_{th} are the low and high threshold voltages respecitvely.

1. The most common implementation of logic gates is with CMOS (complementary metal oxide semiconductor) made from PMOS and NMOS transistors. PMOS and NMOS transistors are

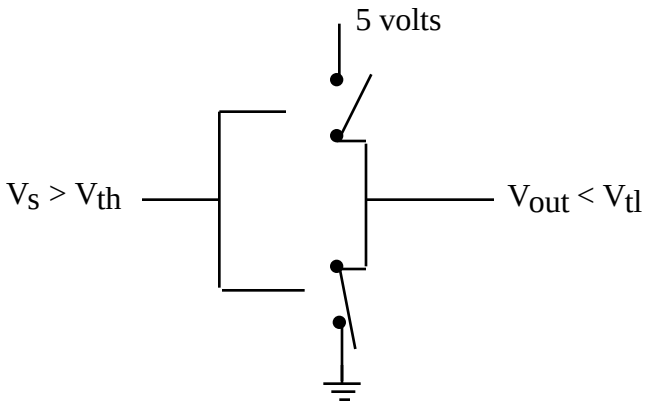
"magical" circuit elements that - at least ideally - can be modelled with switches as follows



So all we have to do to build a CMOS inverter is put together a PMOS and NMOS as follows

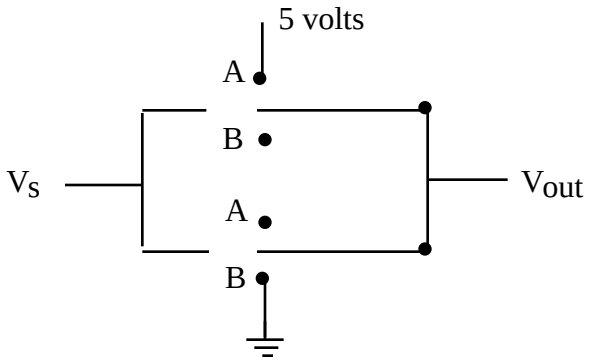


When $V_S \geq V_{th}$ this circuit can be modelled as follows



Draw the corresponding circuit model when $V_S \leq V_{tl}$

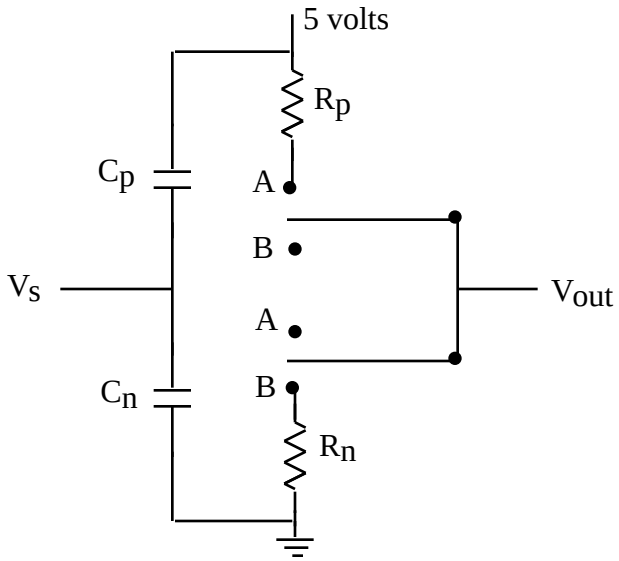
2. Redrawing the circuit of Problem (1) with a ganged switch we have



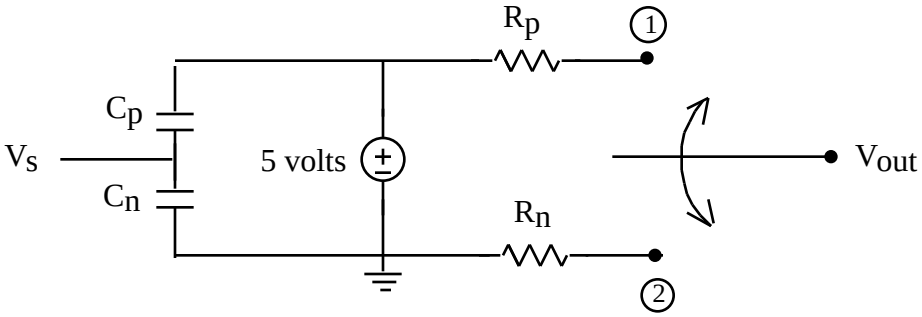
Redraw this circuit for when

a. $V_s \geq V_{th}$
b. $V_s \leq V_{tl}$

3. The models in Problems (1) and (2) are great for seeing the basic operation of a logic gate but to calculate how long it takes a gate to transition from one voltage level to another we need to include the equivalent capacitances and resistances of the PMOS and NMOS transistors as follows

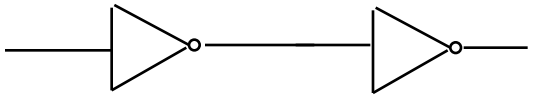


which we can redraw as follows

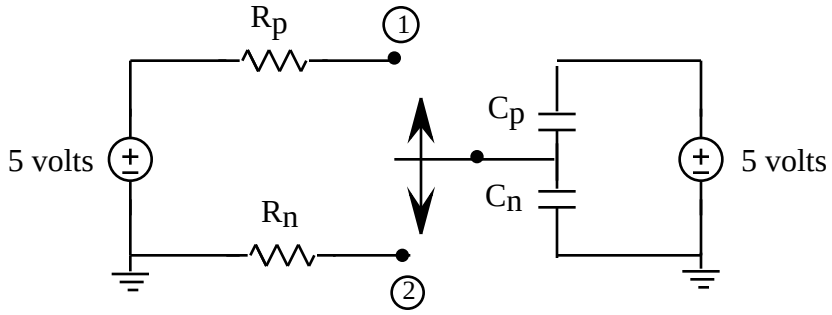


Redraw this circuit with R_p = 1K, C_p = 2 fF, R_n = 1K and C_n = 2 fF. Note that f stands for femto and is equal to 10^{-15}

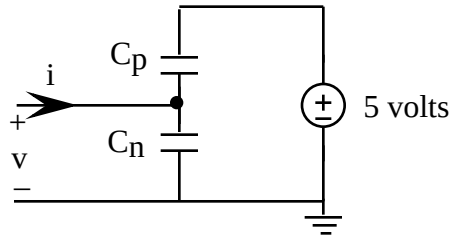
4. If we connect two CMOS inverters together as follows



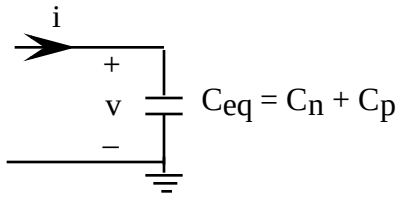
Then at the interface between these two logic circuits we have



Show that

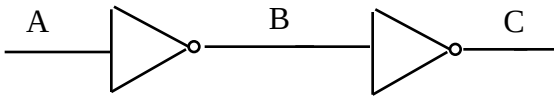


is equivalent to a single capacitor of value $C_{eq} = C_n + C_p$ as follows

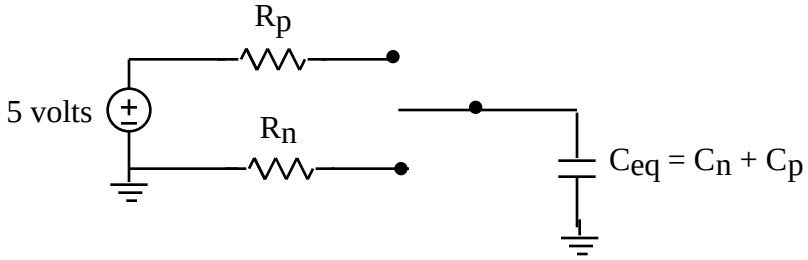


Hint - write the node equation for i.

5. From Problem (4) we have that the interface between two CMOS inverters as follows

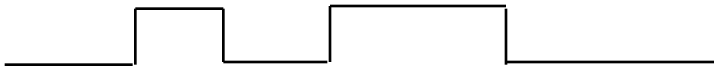


is given by



Now if R_p = 1K, C_p = 2 fF, R_n = 1K and C_n = 2 fF

a. Draw timing diagrams for B and C if A looks as follows

A 

b. Make use of your results from Problem (4) to draw an equivalent circuit for the interface between the two gates
c. Draw the equivalent circuit when $V_s \geq V_{th}$
d. Draw the equivalent circuit when $V_s \leq V_{tl}$