ECE 204 - THE VERY BASICS - INVESTIGATION 4
BASIC LOGIC GATES

FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

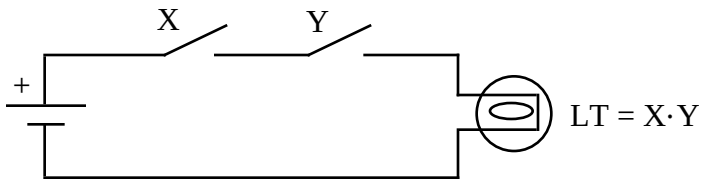
Up to now we've been making all our logic circuits with switches. But in the real world of course virtually all logic circuits are made from integrated circuits. The objective of this Investigation is to describe the operation of basic integrated circuit logic gates and show how they can be modeled with switches.

1. We begin with a review problem. Find the equation for LT with the following truth table

X	Y	LT
L	L	L
L	H	H
H	L	H
H	H	L

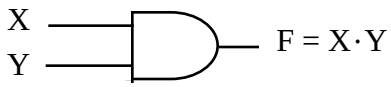
as a sum of minterms.

2. This problem introduces AND gates. Up to now we've built circuits to implement the AND logic function by putting switches in series as follows



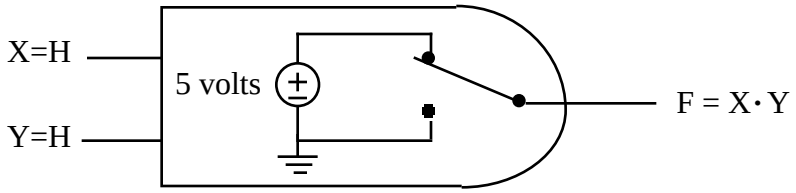
in which LT has a voltage across it and is ON only when both switches are CLOSED - only when both X=H and Y=H.

An alternate way to implement the AND logic function is with integrated transistor circuits we refer to as **AND Gates** as follows



X	Y	F
L	L	L
L	H	L
H	L	L
H	H	H

in which the output F is high (is equal to 5 volts) only when both X = H and Y = H just like in series switching circuits. Note that we can model what's going on inside the integrated circuit AND Gate with the following *equivalent circuit*

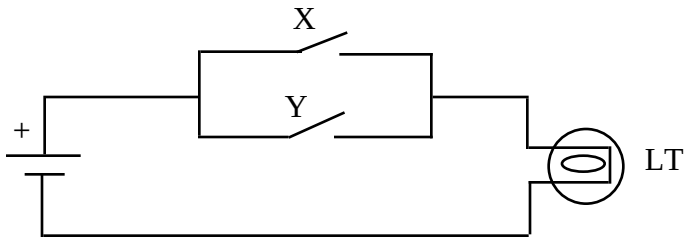


consisting of a switch that connects F to the positive terminal of the 5 volt source when X=Y=H as shown and connects F to ground otherwise. Note that in contrast to the series switching circuit above, X and Y together control the one equivalent switch of the AND gate. Draw the equivalent circuit for the AND gate when

a. X=H and Y=L
b. X=H and Y=H

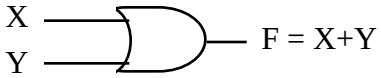
3. Draw a sample timing diagram for an AND gate with inputs X and Y and output F

4. This problem introduces the OR gate. Up to now we've obtained the OR logic function by putting switches in parallel as follows



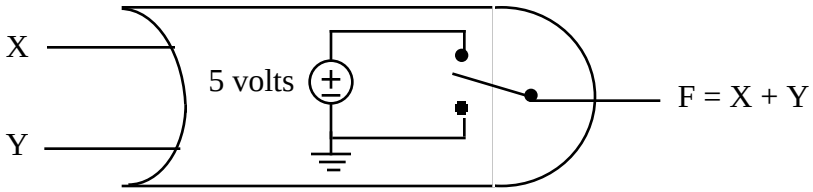
with LT = X+Y = (X OR Y). Note in particular that X and Y control separate switches.

An integrated circuit implementation of the OR logic function with an **OR Gate** as follows



X	**Y**	**F**
L	L	L
L	H	H
H	L	H
H	H	H

with F having the same truth table as LT in the above parallel switching circuit. Note that we can model what's going on inside the integrated circuit OR Gate with the following *equivalent circuit*

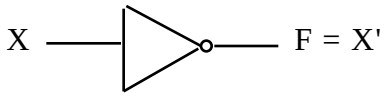


consisting of a switch that connects F to the positive terminal of the 5 volt source when X=H or Y=H and connects F to ground when X=Y=L. Note that in contrast to the series switching circuit above, X and Y together control the one equivalent switch of the OR gate. Draw the equivalent circuit for the OR gate when

a. X=L and Y=L
b. X=H and Y=L

5. Draw a sample timing diagram for an OR gate with inputs X and Y and output F

6. This problem introduces the **NOT** or **INVERTER** logic element. An integrated circuit implementation of the **NOT** or **INVERTER** logic function as follows

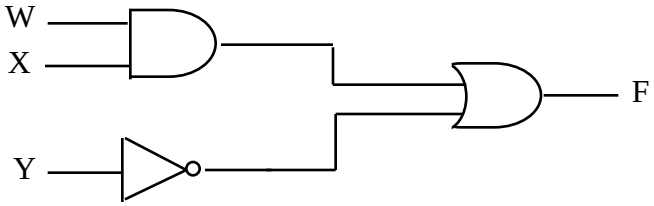


X	**F**
L	H
H	L

is a circuit whose output is the complement of its input. Note that the circle at the end of the triangle is what indicates the NOT function. Draw equivalent circuits like those you drew in Problems (2) and (4) for an INVERTER with
   a. X = L
   b. X = H

7. Draw a sample timing diagram for an INVERTER with input X and output F

8. What really makes logic gates so much more important and useful than the switches of the first three Investigations is the fact that they can be connected together like in the following example



with the outputs of the AND gate and INVERTER determining the input and therefore the output of the OR gate

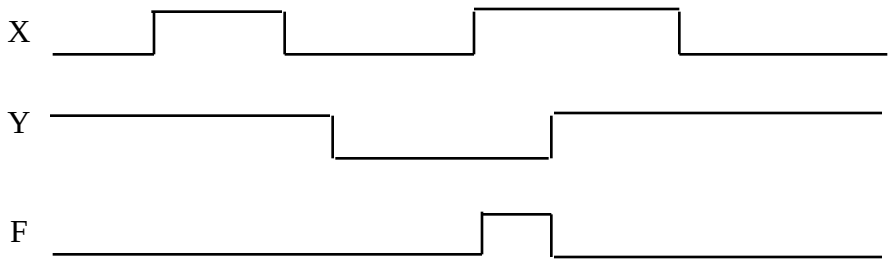
   a. Find the logic equation for F
   b. Draw an equivalent circuit like you did in Problems (2), (4) and (5) for W=L, Y=L and X=H

9. Draw logic diagrams like the one in Problem (8) for the following logic equations
   a. $F = W \cdot X + Y$
   b. $F = (W + X') \cdot Y$

10. Draw the logic diagram for a circuit with the following truth table

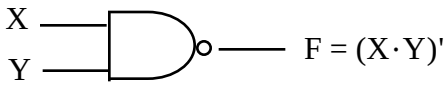
X	**Y**	**F**
L	L	L
L	H	H
H	L	H
H	H	L

11. Draw the diagram of a logic circuit that has the following timing diagram

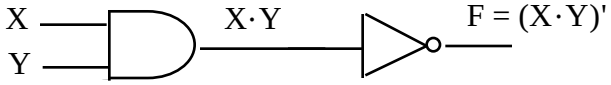


12. Besides the basic AND-OR-INVERTER (AOI) gates, we often seen other simple gates like NAND, NOR and EXCLUSIVE-OR gates

    a. **NAND** gates (**N**OT **AND** gates) as follows

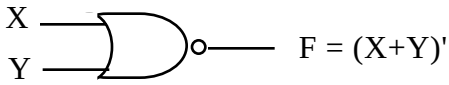


    are functionally equivalent to AND gates followed by INVERTERS as follows

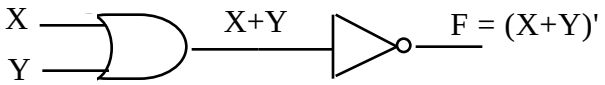


    Write the Truth Table for a NAND gate

    b. **NOR** gates (**N**OT **OR** gates) as follows

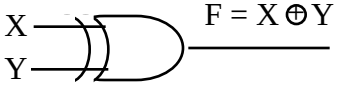


    are functionally equivalent to OR gates followed by INVERTERS as follows



    Write the Truth Table for a NOR gate

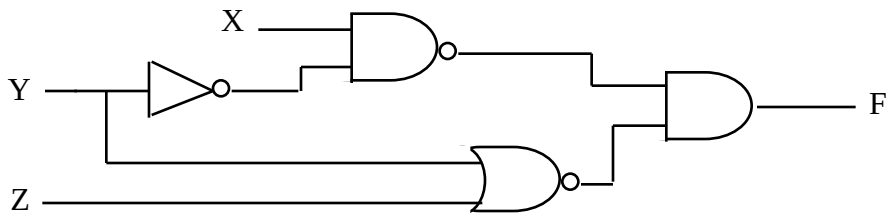
    c. **EXCLUSIVE-OR** gates with Truth Table as follows



X	**Y**	**F**
L	L	L
L	H	H
H	L	H
H	H	L

    How is the EXCLUSIVE-OR gate different from the *regular* (inclusive) OR gate. **Memorize** the difference.

13. Find an equation for F in the following circuit



14. Up to now all our gates have only had two inputs. But gates with more than two inputs are also very common.
    a. Draw the logic symbol for a 3-input AND gate and then write out its Truth Table
    b. Draw the logic symbol for a 3-input OR gate and then write out its Truth Table

15. Find and draw the pin diagram for 7400 quad 2-input NAND IC. Note that IC's with up to around twenty gates are referred to as SSI (small scale integration) IC's.

16. Suppose we wish to monitor the operation of an engine. Design a logic circuit to sound an alarm A when the signal from the pressure gauge is too low (L) or the signal from the temperature gauge is too high (H)