# ECE 204 - COUNTERS - INVESTIGATION 22
# SYNCHRONOUS COUNTERS - PART II

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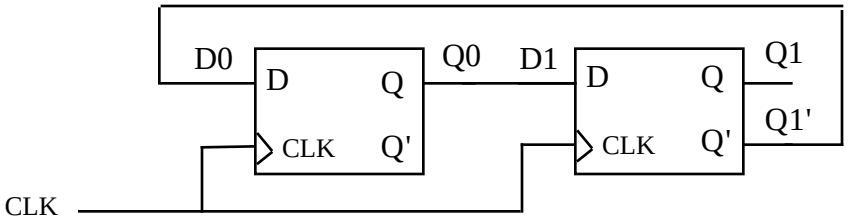
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

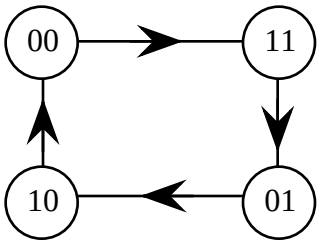
In the last Investigation we showed how to analyze synchronous counters. We showed in particular how to draw timing diagrams, how to set up next state tables and how to draw state diagrams. The main objective of this Investigation is to introduce a method for designing synchronous counters.

1. We begin with a review problem. Given the following synchronous counter




   a. Find equations for D0 and D1
   b. Find the next state table
   c. Draw the state diagram

2. Given the following state diagram




   a. Find the next state table
   b. Draw the circuit timing diagram assuming all the flip-flops are initially cleared

3. The objective of this problem is to illustrate how to design counters like the ones we've been analyzing. Suppose in particular we want to build a 2-bit counter with two D flip-flops that has the following next state table

| Q1 | Q0 | Q1* | Q0* |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

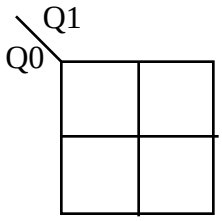
   a. Draw a state diagram for this counter

b. Since the next state of each flip-flop is determined by its inputs we begin our design by inserting columns in our table for the values of D1 and D0 as follows

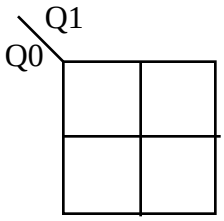
| **Q1** | **Q0** | **D1** | **D0** | **Q1*** | **Q0*** |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | | | 1 | 1 |
| 1 | 0 | | | 0 | 1 |
| 1 | 1 | | | 0 | 0 |

that will make the flip-flops go to the next state Q1*Q0* at the clock. Complete the table

c. Make use of your table in part (b) to obtain equations for D1 and D0 in terms of Q1 and Q0. Hint - use Karnaugh maps as follows to obtain equations for D1 and D0




D1 =




D0 =

d. Make use of your results in part (c) to draw the logic diagram of your counter

4. Generalizing on the design example in Problem (3) we have the following algorithm for designing counters with D flip-flops

   (1) Write out the next state table for the counter
   (2) Add columns for the flip-flop inputs to generate the desired next states
   (3) Make use of your augmented table in part (2) to generate equations for the D's in terms of the Q's
   (4) Use combinational logic to realize the logic equations for the D's

   Now use this algorithm to realize a 3-bit synchronous binary up-counter with D flip-flops. Use PALS as introduced in Investigation 15 for the combinational logic

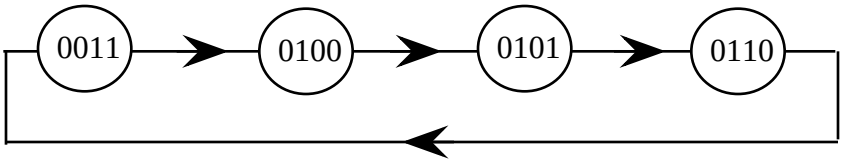
5. The objective of this problem is to design a synchronous divide by 5 counter that counts as follows

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 0 \rightarrow 1 \cdots$$

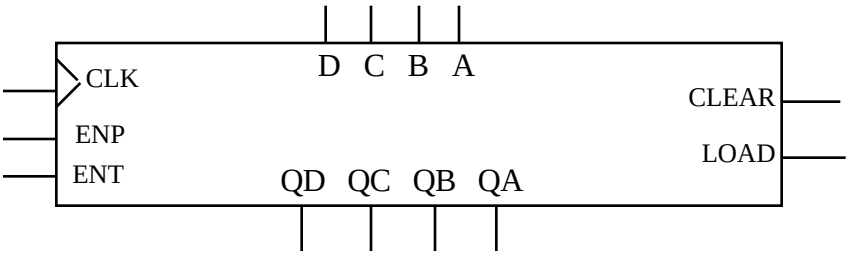
   a. First use D flip-flops together with AOI gates for the combinational logic
   b. Then use D flip-flops together with a PAL for the the combinational logic

6. Design a 2-bit gray code counter with D flip-flops. Note that Gray codes were introduced in Investigation 11.

7. Up to now we've been designing counters from scratch. But it's also possible to make use of IC's to facilitate the design. Realize the following counter




with a 74LS163 as follows




| ENP | ENT | CLEAR | LOAD | CLK | FUNCTION |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | ↑ | hold |
| 1 | 1 | 1 | 1 | ↑ | increment |
| x | x | 0 | 1 | ↑ | clear |
| x | x | 1 | 0 | ↑ | load |

Note that both clear and load are synchronous functions on this chip. And that

(1) Increment means to add 1 to QD QC QB QA
(2) Load means to transfer the input DCBA → QD QC QB QA

Hint - make DCBA = 0011