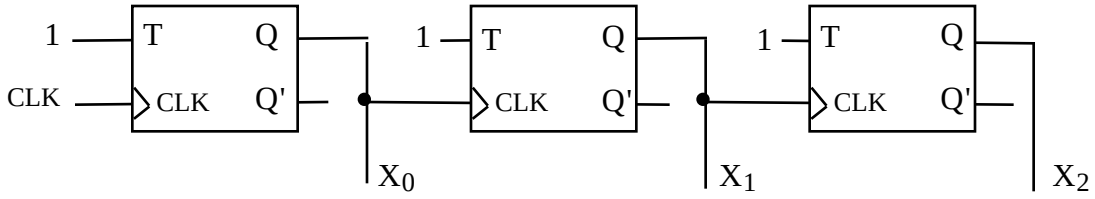
ECE 204 - COUNTERS - INVESTIGATION 21
SYNCHRONOUS COUNTERS - PART I

FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

In the last Investigation we introduced ripple counters like the following

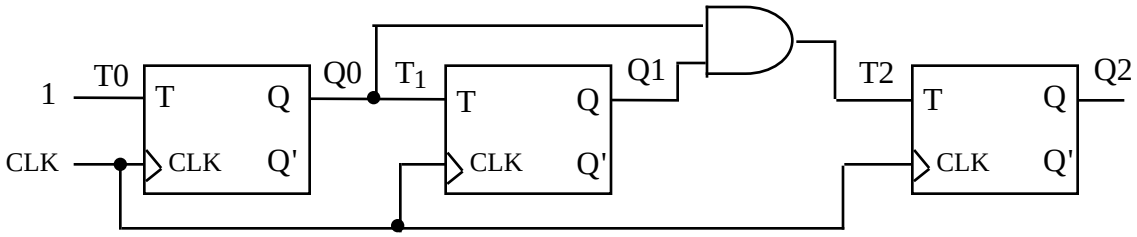


These counters are said to be **asynchronous** sequential circuits because each flip-flop has to wait for the one before it to change before it can change. So the counter cannot reach a new state until the changes caused by the clock pulse CLK have *rippled* all the way through the circuit. Now ripple counters are "ok" but in general sequential circuits are easier to design, easier to troubleshoot and run faster when they're **synchronous** - when all the flip-flops are connected directly to the same clock CLK and therefore all change state at the same time. The main objective of this investigation is to analyze some synchronous counters.

1. We begin with a review of flip-flop equations
   a. Write out the function table for D flip-flops
   b. Write out the function table for JK flip-flops
   c. Write out the function table for T flip-flops

2. What is the difference between synchronous and asynchronous sequential circuits

3. Given the following 3-bit counter

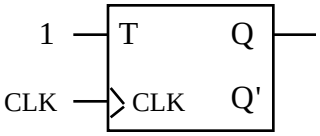


   a. Is this counter synchronous or asynchronous. How can you tell
   b. Obtain equations for T0, T1 and T2
   c. Make use of your equations in part (b) to construct a next state table for this counter as follows

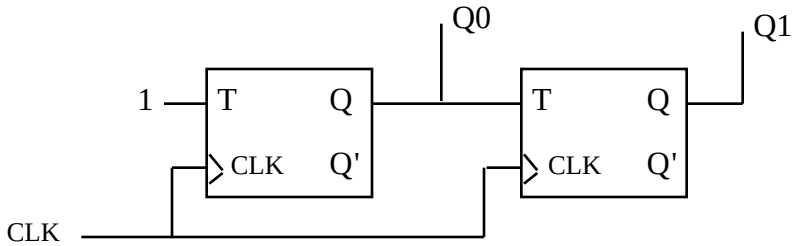
Q2	Q1	Q0	T2	T1	T0	Q2*	Q1*	Q0*

d. Construct a state diagram for this counter
e. Is this an up-counter or down-counter. How can you tell

4. Given the following T flip-flop



a. Draw the timing diagram for Q
b. Why do we call this a divide-by-2 counter
c. Verify that the following logic circuit is a synchronous divide-by-4 counter



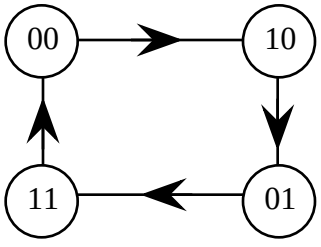
d. Design a divide-by-8 synchronous counter
e. How would you design a divide-by-2^n counter. How many flip-flops would it take

5. Given the following next state table

Q_1	Q_0	Q_1*	Q_0*
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

a. Draw the state diagram
b. Draw the timing diagram assuming all flip-flops are initially cleared

6. Given the following state diagram



a. Find the next state table
b. Draw the circuit timing diagram assuming all the flip-flops are initially cleared