ECE 204 - COUNTERS - INVESTIGATION 20
RIPPLE COUNTERS

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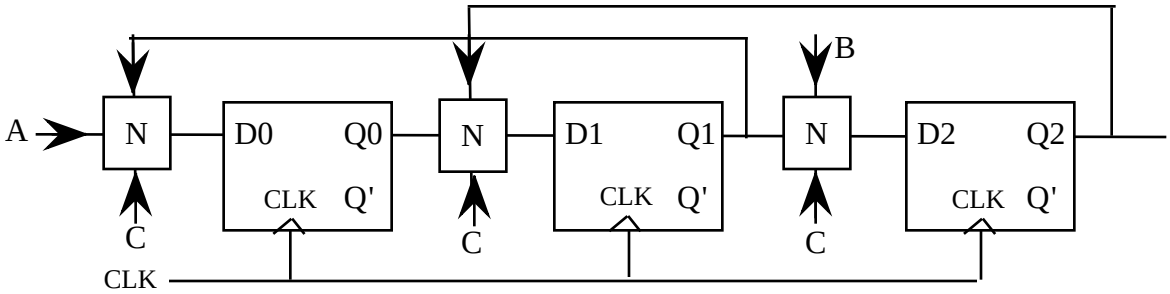
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

Now that we've gotten our feet wet with combinational circuits and with flip-flops we can start putting them together to form what we call **sequential circuits**. The main objective of this and the next two Investigations is to introduce a special class of sequential circuits we call counters.

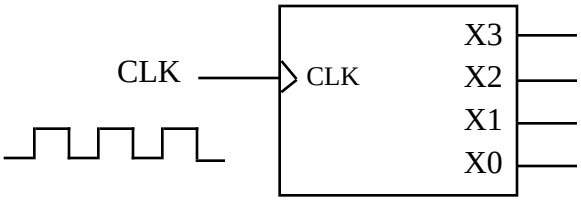
1. We begin with a review problem on flip-flops. Write out the function tables for each of the following flip-flops
   a. D flip-flops
   b. JK flip-flops
   c. T flip-flops

2. The objective of this problem is to review shift registers. Design a circuit N so the following shift register



   will Shift Right if C=0 and Shift Left if C=1. Note that A is the input when the shift register is shifting right and B is the input when its shifting left

3. Now for counters. Counters are sequential circuits of the following form

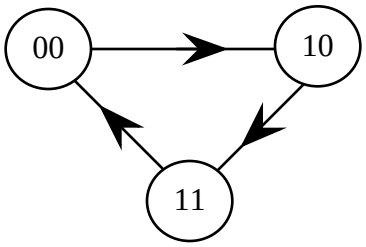


   that produce specified output sequences as the clock runs. A 4-bit **binary counter up-counter** for example will generate the following sequence of outputs

$$X_3X_2X_1X_0\text{: } 0000 \rightarrow 0001 \rightarrow 0010 \rightarrow \cdots$$

   as it counts from 0 to 15
   a. How high can a 10-bit binary counter count
   b. What are the outputs of a 3-bit binary counter that starts at 0 and counts by 2

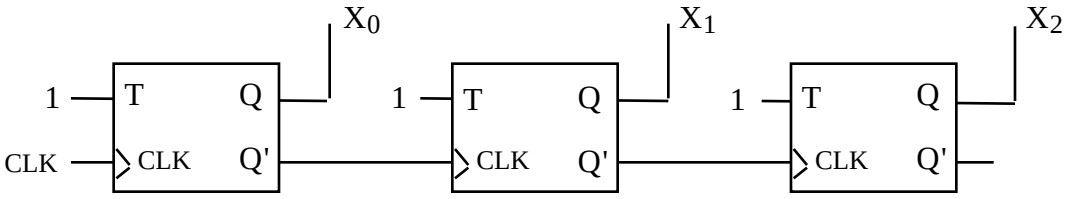
4. The objective of this problem is to introduce **state diagrams** of counter circuits as follows



Such diagrams are helpful because they give us graphical pictures of what's happening to the flip-flops after each clock pulse as the counter counts. Given that the two bit number in each circle is the value of Q1Q0

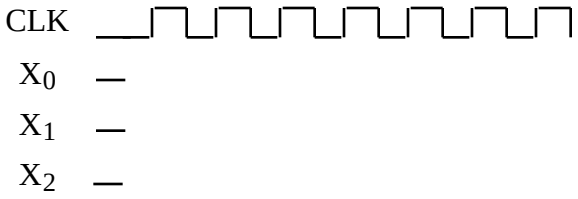
a. Write out the next state table for this counter
b. Draw a timing diagram for the counter

5. The objective of this problem is to introduce ripple counters by analyzing the following 3-bit binary ripple counter



Note in particular that the clock is only connected to the first flip-flop

a. Complete the following timing design for at least the first ten clock pulses. Hint - first do the timing diagram for X_0, then X_1 and then X_2



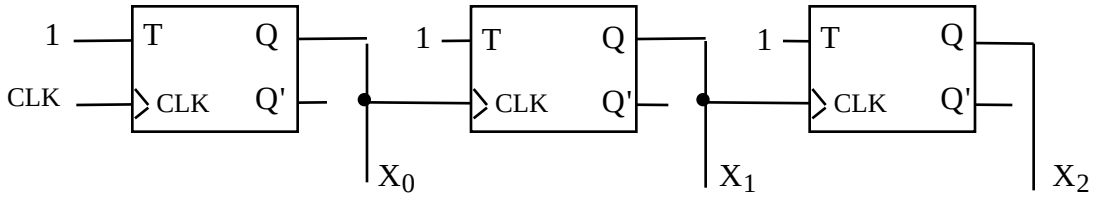
b. Make use of your timing diagram to complete the following **state table** for the next state of each of the flip-flops to verify that our circuit really is a binary up-counter

Present State			Next State		
X_2	X_1	X_0	X_2*	X_1*	X_0*
0	0	0	0	0	1
0	0	1	0	1	0
.			.		
.			.		
.			.		

c. Make use of your state table in part (b) to draw a state diagram of this counter
d. What happens to the counter after it reaches its highest value of $X_2X_1X_0 = 111$
e. Why do we call ripple counters ripple counters

f. Will it take this ripple counter longer to go from 000 → 001 or from 111 → 000. How can you tell

6. Given the following ripple counter - very much like the one in Problem (2)



a. Find the next state table
b. Draw a state diagram
c. How does this ripple counter differ from the one in Problem (3)