ECE 204 - FLIP-FLOPS AND LATCHES - INVESTIGATION 19
FLIP-FLOP EQUATIONS

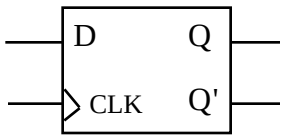
FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

From the last Investigation we know how to build edge-triggered D and JK flip-flops that not only enable us to store 1's and 0's but also transfer stored data from one flip-flop to another. We also observed that D flip-flops are particularly nice since they're so simple. The main objective of this Investigation is to show how to characterize flip-flops by their function tables and excitation equations.

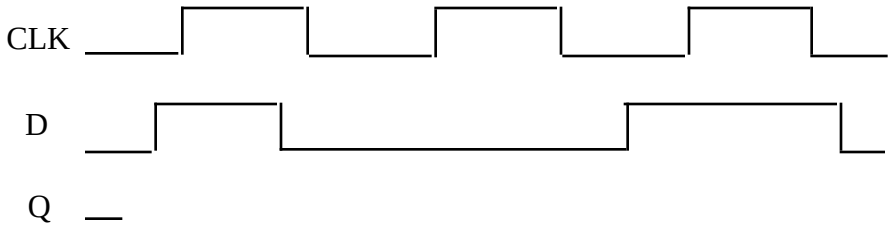
1. Make use of timing diagrams to illustrate the difference between D latches and D flip-flops. Describe how they're different.

2. The objective of this problem is to come up with equations for characterizing positive edge-triggered D flip-flops
   a. In combinational logic we use truth tables to specify the outputs Y of logic gates. For flip-flops we use what we call **function tables** to specify the next state Q* - the value of Q after the rising edge ↑ of the next clock pulse. **Memorize** the definition of function tables. And in particular **memorize** the following function table for D flip-flops

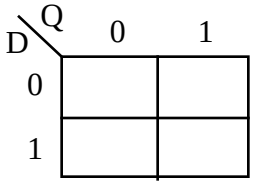


D	CLK	Q*
0	↑	0
1	↑	1

   Then make use of this table to describe in words the relationship between D, Q* and the clock pulse in positive edge-triggered D flip-flops
   b. Make use of the function table in part (a) to complete the following timing diagram of a positive edge-triggered D flip-flop



   c. Now make use of the function table to obtain the Karnaugh Map of a D flip-flop for Q* as follows



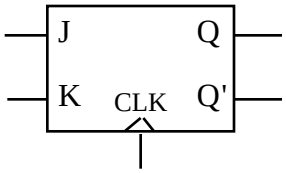
   where the 0's and 1's along the margins are the current values of D and Q and the values

in the squares are the values of Q*

d. Make use of your Karnaugh Map in part (c) to verify that the **excitation** equation for a D flip-flop - the equation for Q* - is given by **Q* = D. Memorize** this relationship.

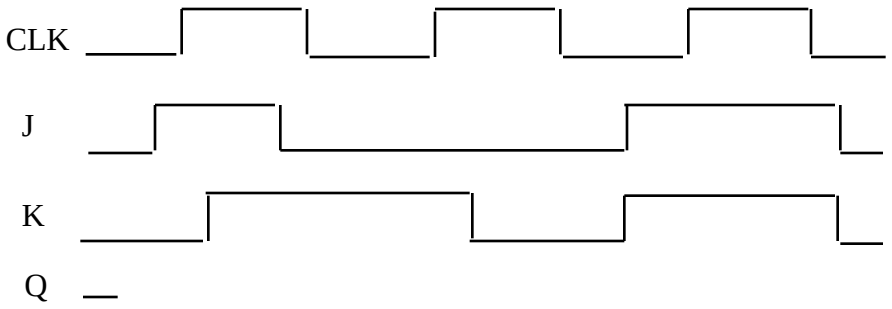
3. Given your results in Problem (2) for positive-edge D flip-flops
   a. Obtain the logic diagram and function table for a negative edge-triggered D flip-flop
   d. Redraw your timing diagram in Problem (1b) if the D flip-flop is negative-edge triggered
   c. How is the excitation equation of a positive edge-triggered D flip-flop related to that of a negative edge-triggered D flip-flop

4. The objective of this problem is to analyze JK flip-flops with function tables as follows



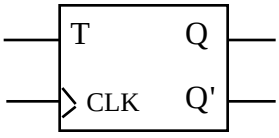
J	K	CLK	Q*
0	0	↑	Q
0	1	↑	0
1	0	↑	1
1	1	↑	Q'

   a. **Memorize** the function table for JK flip-flops. Then make use of it to describe in words the relationship between J, K, Q* and the clock pulse
   b. Make use of the function table to complete the following timing diagram for a positive edge-triggered JK flip-flop



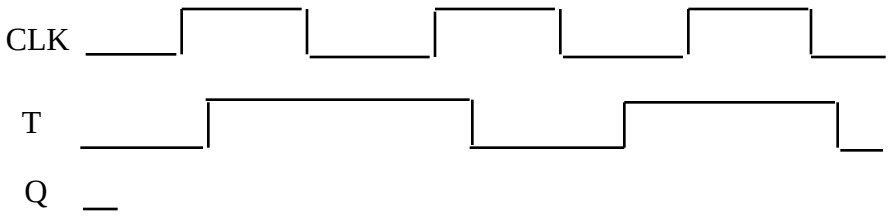
   c. Redraw your timing diagram in part (b) if the JK flip-flop is negative-edge triggered
   d. Make use of the function table to obtain the Karnaugh Map for Q* for a positive edge-triggered JK flip-flop. Remember that Q is the state of the flip-flop just before the rising edge of the clock pulse and Q* the next state of the flip-flop after the rising edge of the flip-flop.
   e. Make use of your result in part (d) to find the excitation equation for Q*

5. The objective of this problem is to analyze T (Toggle) flip-flops with function tables as follows



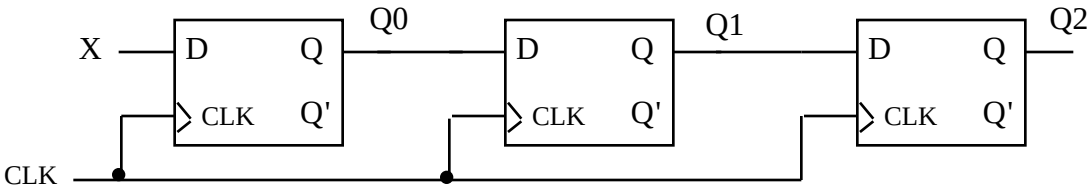
T	CLK	Q*
0	↑	Q
1	↑	Q'

   a. **Memorize** the function table for T flip-flops. Then make use of it to describe in words the relationship between T, Q* and the clock pulse
   b. Make use of the function table to complete the following timing diagram for a positive edge-triggered T flip-flop



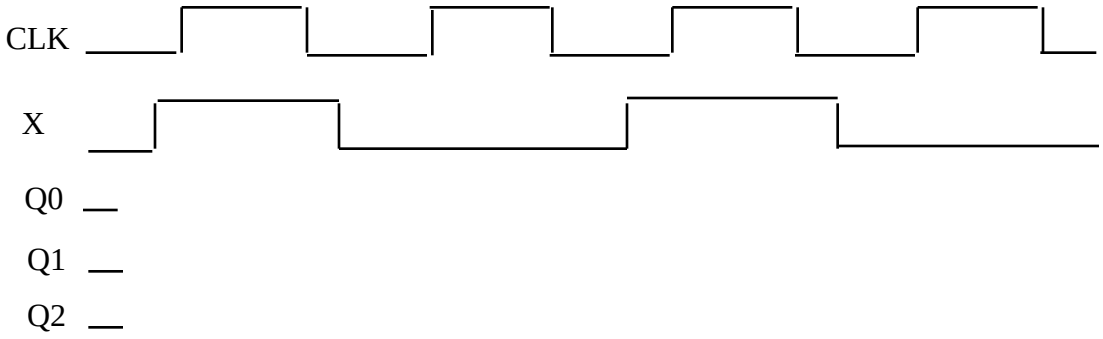
c. Make use of the function table to obtain the Karnaugh Map for Q* for a positive edge-triggered T flip-flop.
e. Make use of your result in part (c) to find the excitation equation for Q*

6. When we connect flip-flops in cascade as follows



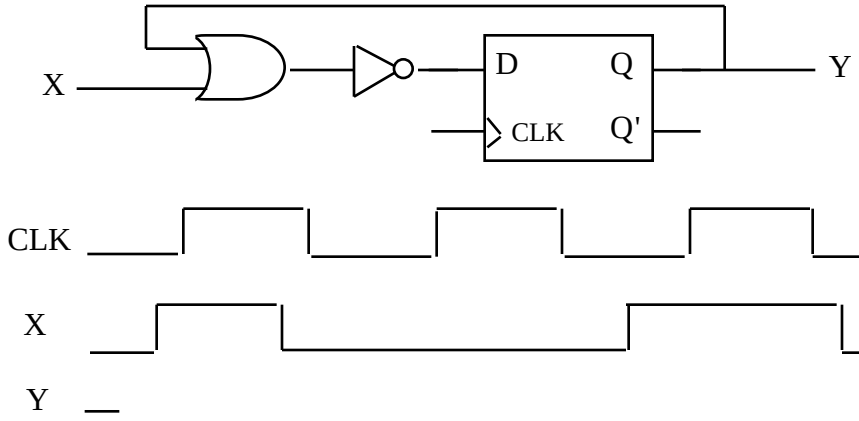
we call the circuit a **shift register**

a. Complete the following timing diagram by first doing Q0 then Q1 and then Q2



b. Describe what's going on in this shift register. Note in particular that the next value of Q is the value of D just before the clock pulse. **Memorize** your result.

7. Complete the timing diagram of the following logic circuit containing combinational gates



Hint - start out by writing the equation for D and then writing out the next state table as follows

X	Q	D	Q*