ECE 204 - FLIP-FLOPS AND LATCHES - INVESTIGATION 18
INTRODUCTION TO FLIP-FLOPS

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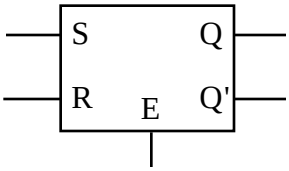
To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

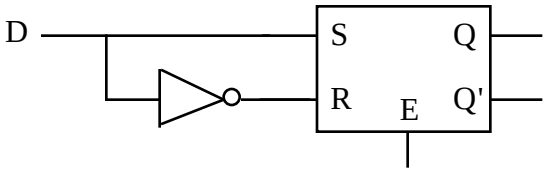
From the last Investigation we know that as long as E=1 the output of an SR latch with level sensitive enabling as follows



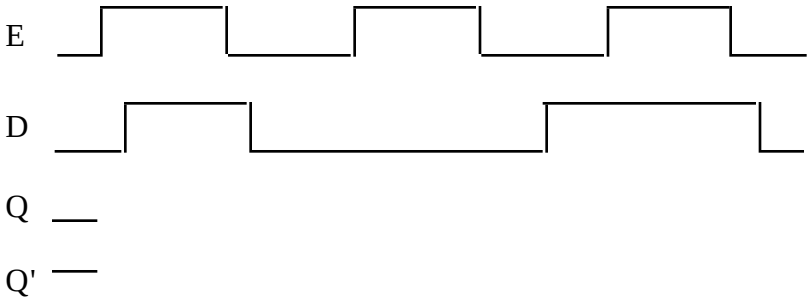
will change as a function of S and R. But as soon as we make E=0 then the last value of Q will be saved. Now at first blush SR latches with level sensitive enabling look great. But in fact they have a major problem. The objective of this Investigation is to point out this problem and then show what we can do about it.

1. From the introduction we know that the output of an SR latch will be saved when E=0. How does this differ from what happens in combinational circuits with enables.

2. The objective of this problem is to introduce the D latch as follows

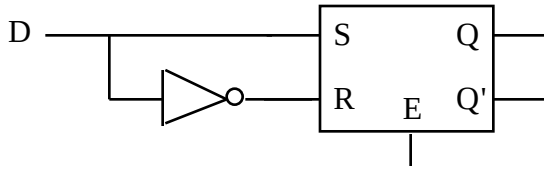


   a. What are two advantages of D latches over SR latches
   b. Complete the following timing diagram for a D latch

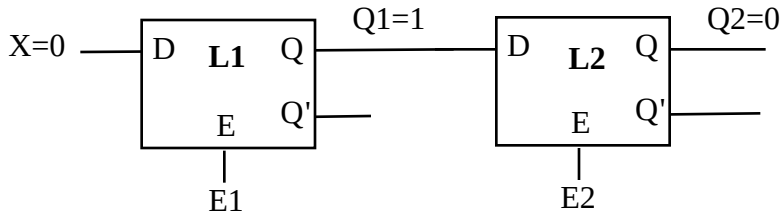


   c. Write out the truth table for the D latch with Q as a function of D and E
   d. We say a latch is **transparent** when it's enabled - when the output can change in response to changes in its input. When is the D latch transparent

3. From Problem (2) we know that the input to a D latch like the following

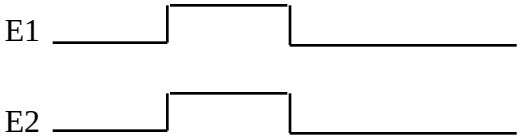


will be stored when E=1 and will stay stored when E=0. This is all great and useful in some applications but latches have a major limitation when we try to transfer data from one to another in a circuit like the following

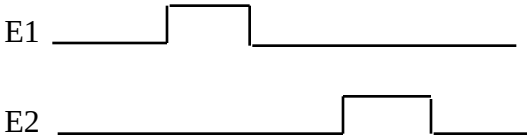


where we would like to store X=0 in latch L1 and Q1=1 in latch L2

a. What will happen - what will end up being stored in the latches - if we simply enable them both at the same time as follows

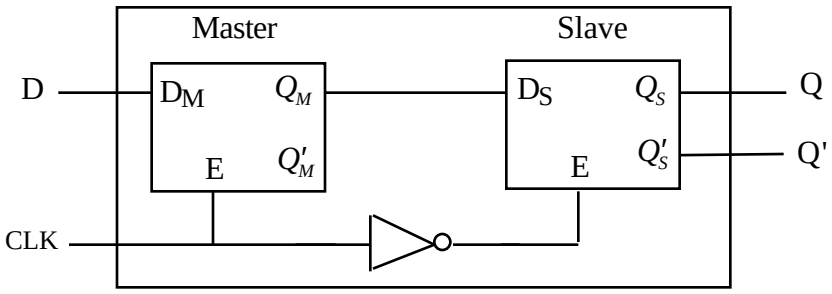


b. What will happen if we enable the latches as follows



c. From parts (a) and (b) we have two schemes that don't give us the desired data transfer. Make use of what you learned to come up with a timing diagram for the enables that will give us the desired data transfer

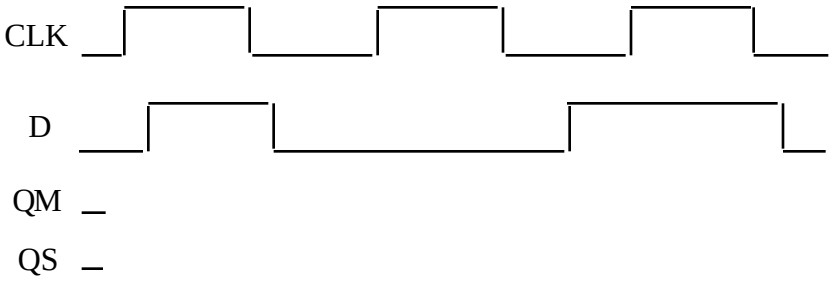
4. From Problem (3) we see that we can transfer data from one D latch to another. But each latch requires its own separate enabling signal. This is a big pain to implement in small circuits and virtually impossible to do in larger circuits. So we need to modify our latches so we can use a common enable signal - a common **clock** - for the whole system. One way this can be done is to put two D latches together as follows



to form what we call a **master-slave D flip-flop** with **clock** CLK. When the clock is

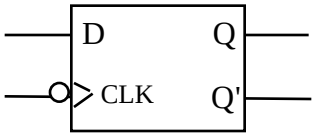
HIGH the master will store the value of D. And when the clock goes LOW the master will transfer its stored value to the slave.

a. Draw the following timing diagram for the master-slave D flip-flop



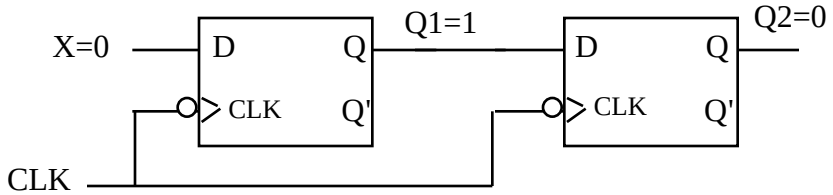
b. Make use of your result in part (a) to determine where in the clock cycle the value of D reaches the output at Q

c. Since the output Q of our master-slave D flip-flop changes during the falling edge of the clock pulse, we say it's a **negative edge-triggered** D flip-flop with symbol as follows



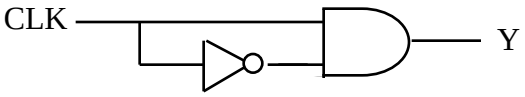
The triangle tells us that the flip-flop is edge-triggered and the bubble tells us that it's negative edge-triggered.

Now explain in words how the value of X can be transferred to Q1 and the value of Q1 transferred to Q2 at the falling edge of the common clock CLK in the following circuit made from master-slave D flip-flops

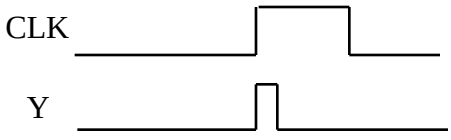


5. From Problem (4) we know that master-slave flip-flops solve the problem of transferring data from one flip-flop to another. But as it turns out there's another solution to this problem with what are called **edge-triggered flip-flops** that are faster and more reliable.

a. The key component of edge-triggered flip-flops is an **edge detecting circuit** like the following

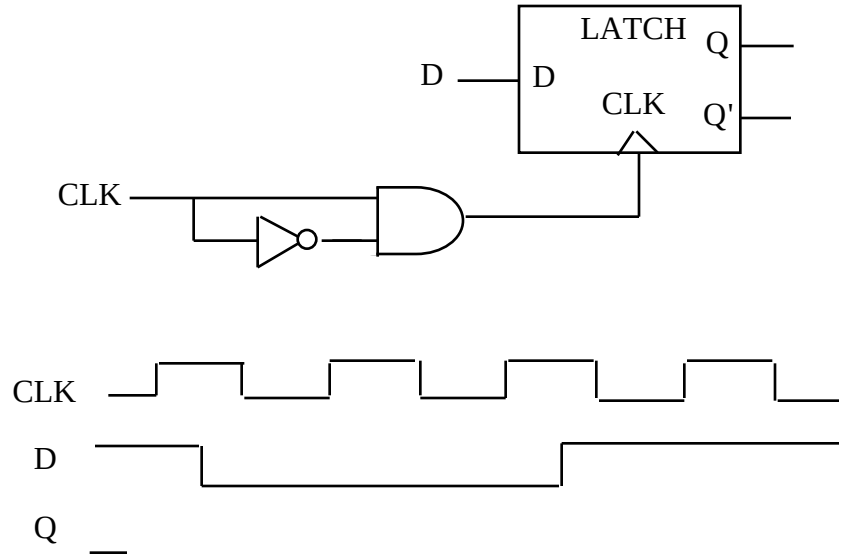


with a timing diagram as follows



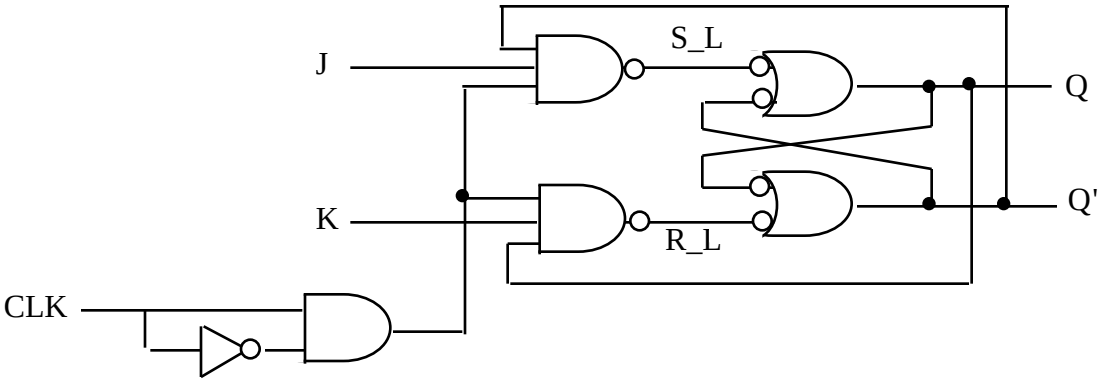
Explain why Y has a small but real pulse when this circuit is built with real IC's with nonzero propagation delays

b. Why do we say that a latch with the edge detecting circuit of part (a) connected to its enable is positive edge-triggered
c. Make use of the timing diagram in part (a) to complete the timing diagram of the following positive edge-triggered D flip-flop



d. Resketch the your timing diagram in part (c) if the latch was negative edge triggered

6. D flip-flops like those in Problem (5) are the simplest and most common flip-flops but there are others that you will see and hear about like JK and T flip-flops. The JK flip-flop is very much like the SR latch except that there are no "not allowed" inputs. Given the following realization of a positive edge-triggered JK flip-flop



a. Draw a timing diagram to illustrate what happens to Q when JK=11
b. Make use of your result in part (a) to describe what happens to Q when JK=11