ECE 204 - COMBINATIONAL BUILDING BLOCKS - INVEST 15
PROGRAMMABLE LOGIC DEVICES

FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

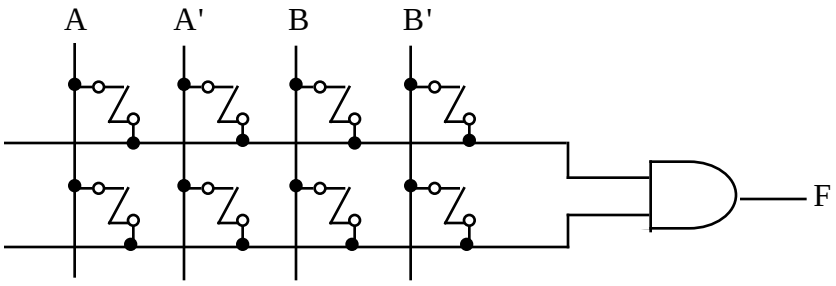
Up to now we've been implementing our combinational logic with AOI gates and MSI circuits like decoders and multiplexers. These circuits are "ok" but the package count can get pretty big. And they can be hard to modify.

But luckily not all is lost. Starting in the late 1970's logic designers began developing programmable logic devices (PLDs) that enable designers to implement arbitrary logic functions. The main objective of this Investigation is to introduce a PLD developed by Advanced Micro Devices (AMD) that they refer to as a PAL.

1. The objective of this and the next several problems is to introduce a general class of logic circuit called **Programmable Logic Devices** (**PLDs**) for realizing logic functions equal to sums of products like the following

   $$F = A \cdot B' + B$$

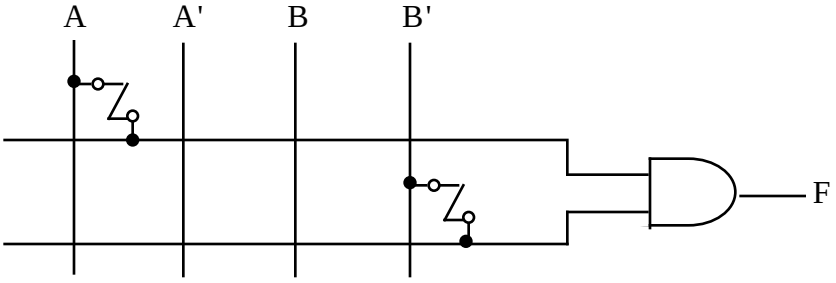
   The objective of this problem is to introduce **AND arrays** used in PLDs like the following



   Note in particular that this circuit has fuseable links (thin wires) as follows

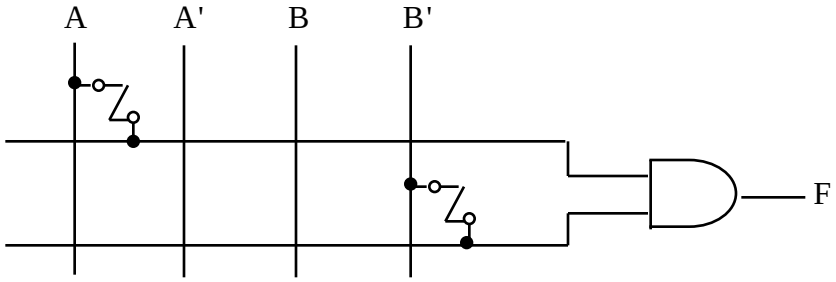
   that are blown by the designer when the PLD is being "programmed".

   a. What is the equation for F in the following circuit if all but the following fuses have been blown

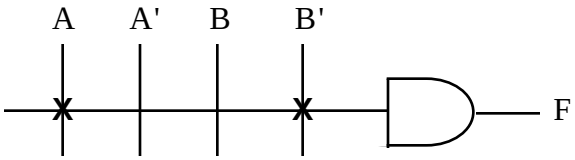


   b. Draw the AND array for realizing $F = A' \cdot B$

2. Since PLDs can easily have up to 16 inputs we clearly need some kind of shorthand notation to indicate which fuses are blown and which aren't in the AND arrays. For the AND array of Problem (1b) as follows

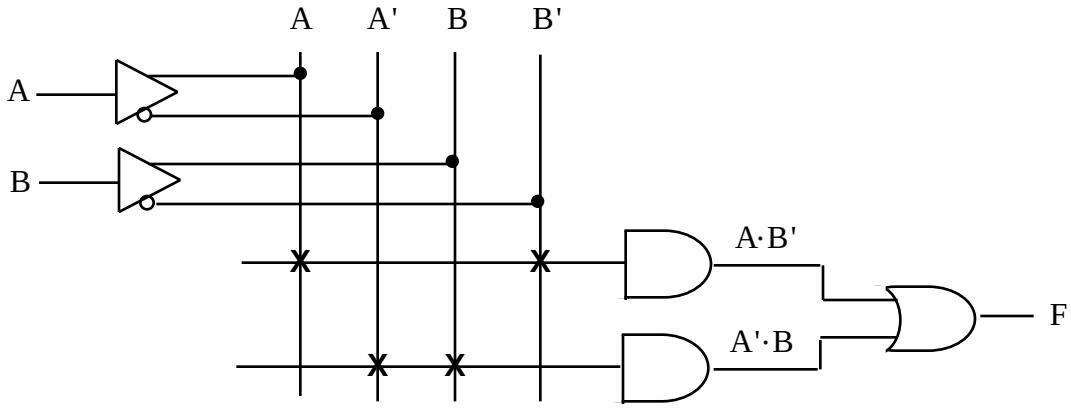


we simply draw the circuit as follows



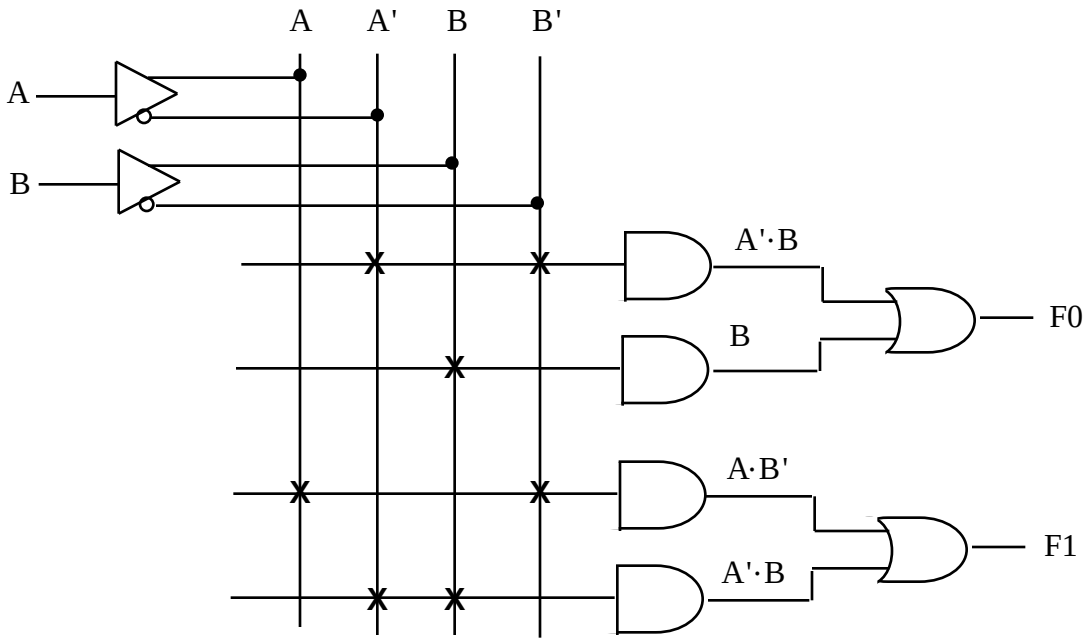
a. What does the presence of an x mean
b. What does no x imply
c. Use this shorthand scheme to realize $F = A' \cdot B \cdot C$ for an AND array with the three inputs A, B and C

3. Now suppose we wish to realize $F = A' \cdot B + A \cdot B'$ with AND arrays. All we need to do is add another AND gate and an OR gate as follows



Note that we have shown the **input buffers** that generate A' and B'.
a. How many fuses did the original array have
b. How many fuses had to be blown to obtain F
c. Use an AND array to realize $F = A \cdot B + A' \cdot B'$

4. From Problem (3) we know how to realize a sum-of-products with an AND array and an OR gate. When we expand such circuits to generate more than one output as follows



then we have a special case of a PLD that we call a **Programmable Array Logic** or **PAL**. Note in particular that PALs are characterized by having AND arrays that are programmable and OR arrays that are fixed.

a. How many fuses were in the original circuit
b. Draw a PAL to realize

$F0 = A + A' \cdot B$

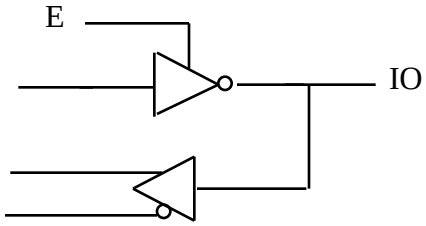
$F1 = A \cdot B' + B$

5. Draw a circuit diagram of a PAL to realize the following Truth Table

I2	**I1**	**I0**	**F1**	**F0**
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

Note that we must include every product term for each output F0 and F1 even when there are repeats.

6. A very nice feature of currently available PALs is that they have programmable outputs as follows



a. Is the IO pin functioning as an input or an output when E=0. Explain how you know
b. Is the IO pin functioning as an input or an output when E=1. Explain how you know

7. One of the real advantages of PALs is that with as few as 20 pins they can have as many as 16 inputs. The price we pay is that outputs are typically the sums of a limited number of minterms.
   a. How many fuses does a PAL have if it has n=10 inputs, m=4 outputs and p=6 product terms for each output.
   b. How many fuses would the PAL in part (a) have if it generated every minterm for each output