ECE 204 - COMBINATIONAL BUILDING BLOCKS - INVEST 14 DATA TRANSFER

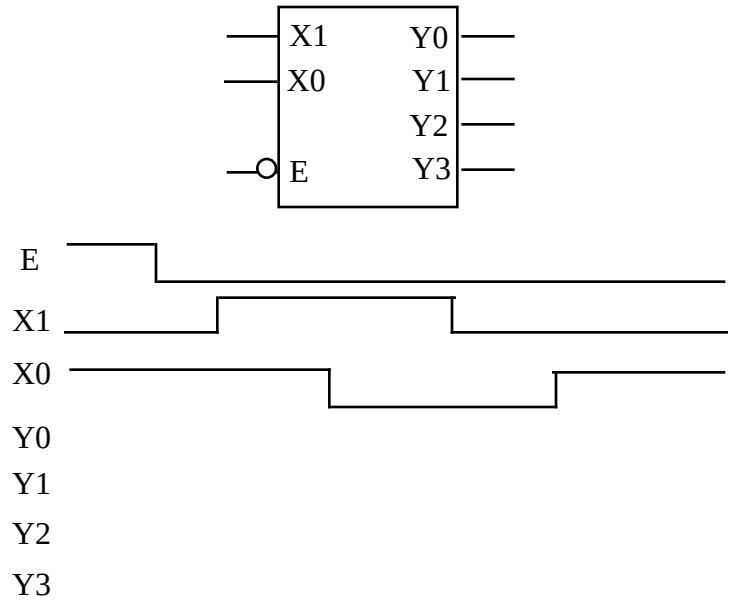
FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

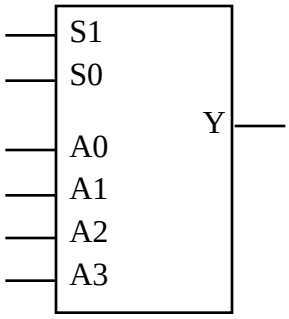
When we look inside digital systems we see two basic kinds of things going on. One of these is information processing like encoding, decoding, adding, subtracting and so on. The other basic thing that's going on is the transfer of data from one place to the other. Clearly we can't have separate wires connecting every pair of logic chips that transfer data. The number of wires would be overwhelming. So what we use are called buses - groups of wires that are shared just like roads and highways are shared.

The main objective of this investigation is to introduce logic circuits that facilitate the use of data transfer on buses. We will first introduce multiplexers and demultiplexers and then circuits with tri-state outputs.

1. We begin with a review problem. Complete the timing diagram for the following decoder



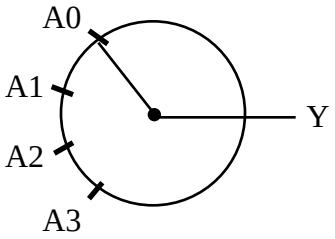
2. The objective of this problem is to introduce multiplexers. The following is the logic diagram and Truth Table of a simple 4-input, 1-bit **multiplexer** which we refer to as a 4-input, 1-bit **MUX**



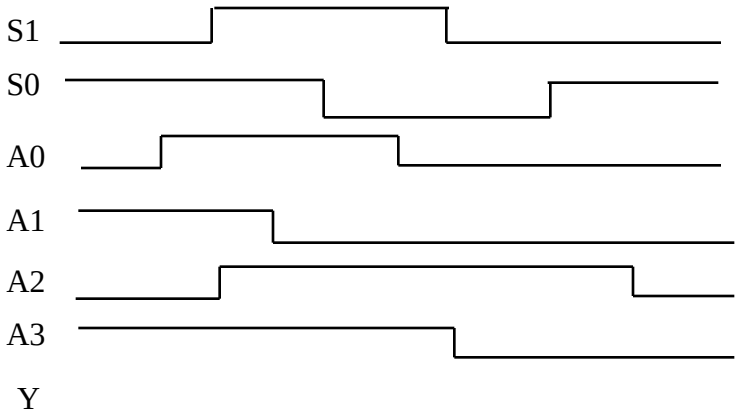
S1	S0	Y
0	0	A0
0	1	A1
1	0	A2
1	1	A3

with data **SELECTS** S1S0.

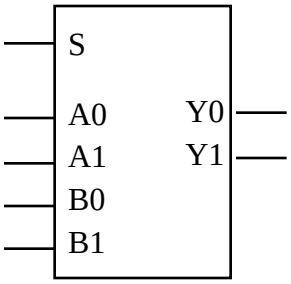
a. Make use of the truth table to describe how the value of Y is related to S1S0 and the values of the A's. **Memorize** how a mux works.
b. Explain how the operation of the following rotary switch



is like the operation of our 4-input, 1 bit MUX
c. Come up with a logic diagram for the MUX using AOI gates. Note that you can use AND and OR gates with more than two inputs.
d. Complete the following timing diagram for the MUX



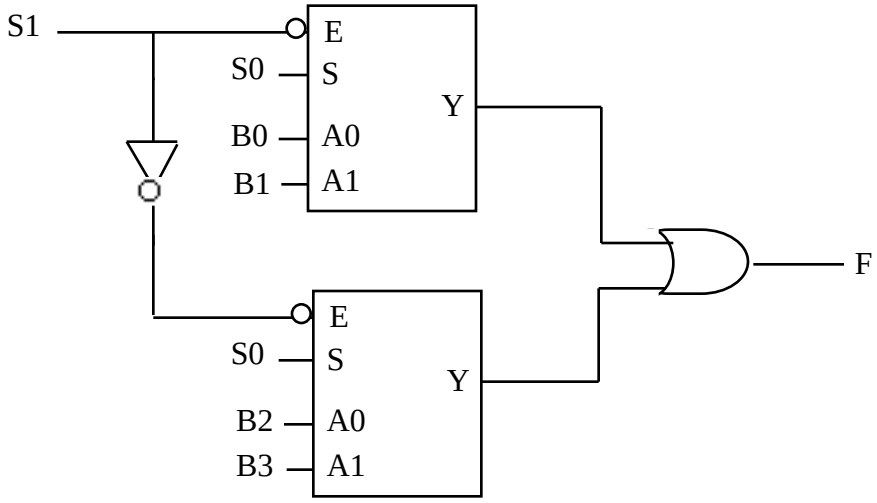
3. From Problem (2) we see that a 4-input, 1-bit MUX enables four incoming signals A0-A3 to share one outgoing line Y. And so the MUX performs the function of a *parallel to serial converter*. Now suppose we have a 2-input, 2-bit MUX with logic diagram as follows



with SELECT S, 2-bit inputs A1, A0 and B1, B0 and shared output lines Y1 and Y0

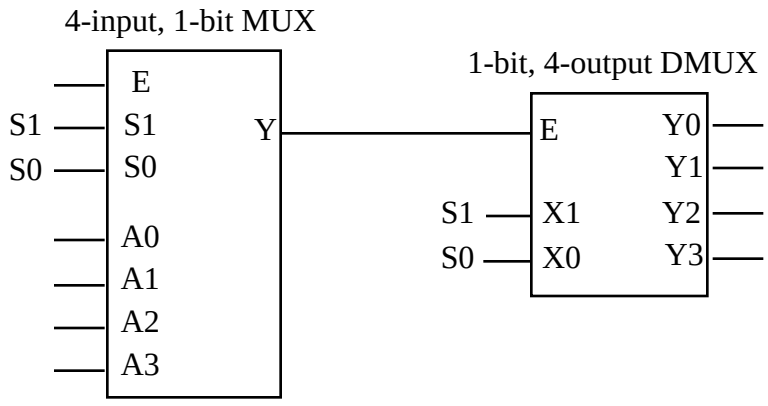
a. Write out a Truth Table for this MUX like the one in Problem (1) if S=0 selects the A's and S=1 selects the B's
b. Design a logic circuit for this MUX with AOI gates

4. Just like for decoders we can make use of enables to put MUX's together to form bigger MUX's as follows



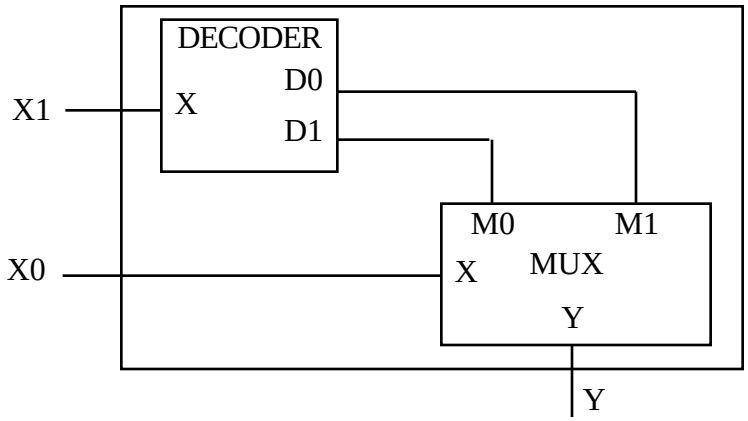
a. Write the truth table for this MUX
b. Make use of your result in part (a) to describe what's going on

5. In the first three problems we saw how MUX's enable signals to share the same BUS. To retrieve individual signals from a BUS we use what we call a **DEMULTIPLEXER** OR **DMUX** like the following circuit where the DMUX is a decoder like those introduced in the last Investigation. Note that both the MUX and DMUX have the same SELECT inputs.

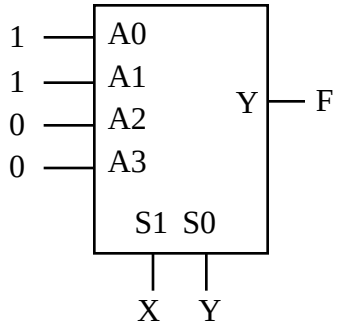


a. Find Y0, . . ., Y3 if S1=1, S0=0, A0=1, A1=0, A2=0, A3=1
b. Find Y0, . . ., Y3 if S1=0, S0=0, A0=0, A1=1, A2=0, A3=1
c. Describe what's going on in this circuit

6. Write out the truth table for the following logic circuit containing a decoder and a MUX



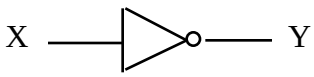
7. Given the following MUX



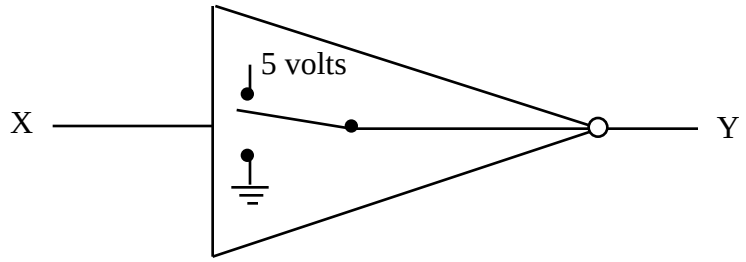
with inputs X and Y and output F

a. Write out the truth table
b. Make use of your truth table to express F as a sum of minterms
c. Describe and then **memorize** how this MUX realizes the equation for F
d. Make use of your result in part (c) to realize $F = X \cdot Y + X' \cdot Y'$ with a MUX

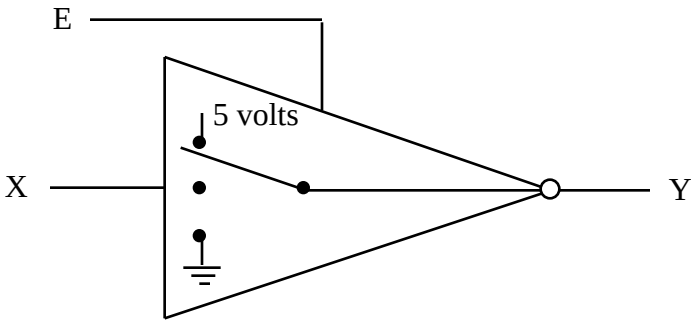
8. The objective of this problem is to show how **tri-state outputs** can be used to implement buses. Up to now all our digital circuits like the following INVERTER



had outputs that could only be H or L as indicated in the following equivalent circuit



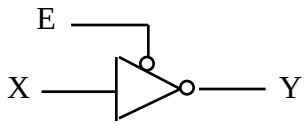
Logic circuits with tri-state outputs on the other hand have three possible outputs - the usual H and L and a third output equal to an open circuit as indicated in the following functional diagram of our tri-state INVERTER



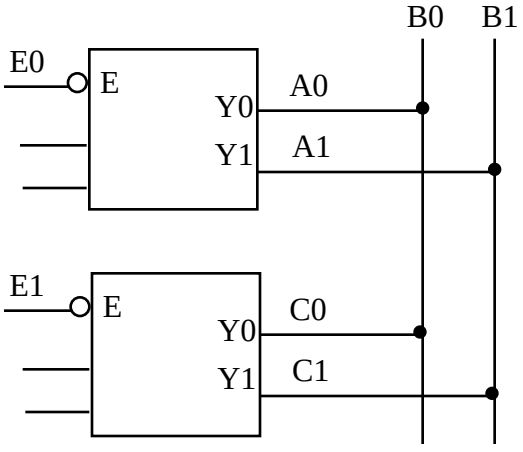
E	X	Y
0	x	Open Ckt
1	0	1
1	1	0

When the ENABLE signal E=1 then Y will equal 0 or 1 as determined by the input. And when E=0 the output is an open circuit

a. Draw a separate equivalent circuit of the tri-state INVERTER for each line of the Truth Table. Be sure to indicate the position of the switch in each case.
b. Write out a Truth Table like in part (a) for the following tri-state INVERTER with active-low enable as follows

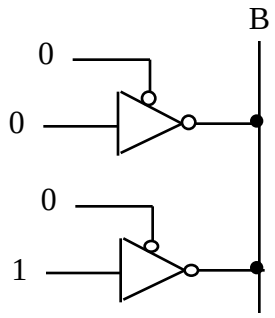


9. Fill in the Truth Table if both logic circuits connected to the following BUS have tri-state outputs



E0	E1	B0	B1
0	1		
1	0		

10. Connecting logic circuits with tri-state outputs to BUSES is great but we must take care that no two circuits are enabled at the same time. What in particular is the problem in the following circuit


B
0
0
0
1