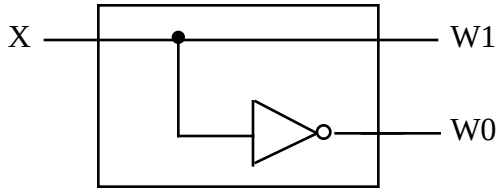
ECE 204 - COMBINATIONAL BUILDING BLOCKS - INVEST 12 INPUTS AND OUTPUTS

FALL 2003 **A.P. FELZER**

To do "well" on this investigation you must not only get the right answers but must also do neat, complete and concise writeups that make obvious what each problem is, how you're solving the problem and what your answer is. You also need to include drawings of all circuits as well as appropriate graphs and tables.

Not long after the introduction of simple logic gates there began appearing larger IC's like decoders and multiplexers that performed more complex functions. The objective of this investigation is to introduce such circuits with a very simple example with a focus on their inputs and outputs. We will introduce *enables* and explore the in's and out's of *active high* and *active low*.

1. We begin with the following very simple logic circuit with one input and two outputs

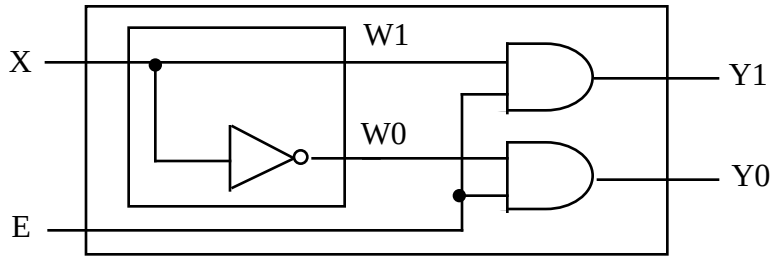


   a. Construct the Truth Table for this circuit as follows

X	W1	W0

   b. Obtain the equations for W1 and W0
   c. Describe in words how W1 and W0 are related to X

2. When we look at the outputs of our simple logic circuit in Problem (1) we see that one of them is always ON. But in the real world we often want to be able to control the circuit in such a way that we can keep all the outputs OFF until we want them. We do this with what we call an **enable**. To implement an enable in the logic circuit of Problem (1) we simply modify it as follows



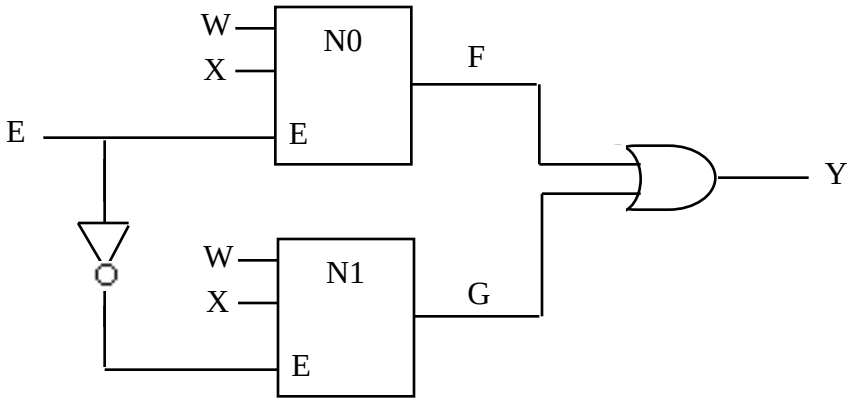
   a. Construct the Truth Table for this circuit with inputs E and X0. **Always** put the enable E in the first column of such Truth Tables as follows

E	X	Y1	Y0

b. Obtain the equations for Y1 and Y0
c. Describe in words how the operation of the circuit depends on the enable E

3. For logic circuits like those in Problem (2) we say that the outputs Y1 and Y0 are **asserted** when the enable E=1 and **not asserted** when E=0. What are the outputs Y1 and Y0 in the logic circuit in Problem (2) when Y1 and Y0 are not asserted. **Memorize** the definition of asserted.

4. Given the following very important application of the enable E



a. Complete the circuit's truth table

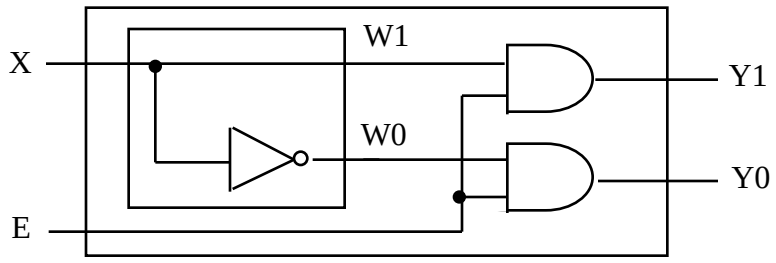
E	Y
0	
1	

b. Describe how the enable E controls the value of the output Y

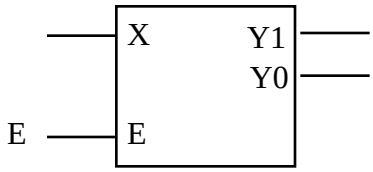
5. Make use of your results in Problem (4) to design a circuit with output Y controlled by the signal C as follows

C	Y
0	W + X
1	W · X

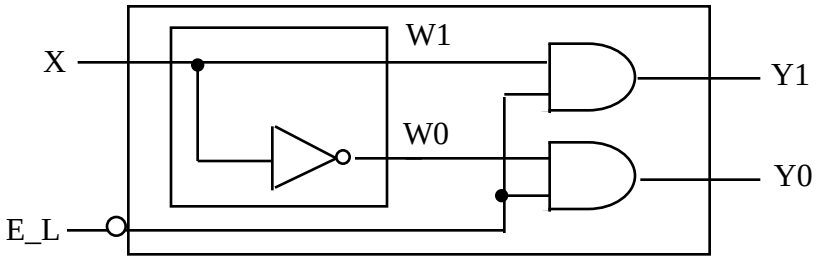
6. The objective of this problem is to introduce what we mean by *active low* and *active high*. We say the enable signal E for the logic circuit in Problem (2) as follows



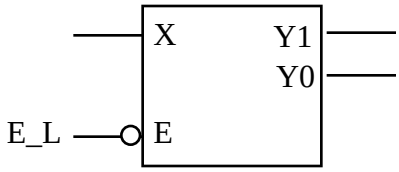
is **active high** because the outputs are asserted when the enable signal is HIGH with E=H (E=1 in positive logic). We draw the corresponding logic symbol for a logic circuit with an active high enable by simply drawing



Now for various insundry reasons logic circuits are often built with **active low** enables - enables that assert the output when the enable is LOW with E=L (E=0 in positive logic). We indicate the corresponding inverters in our logic diagrams with bubbles as follows



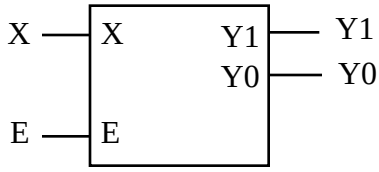
And more generally in our chip diagrams as follows



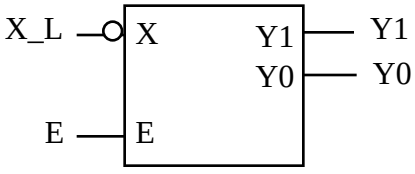
where we have renamed the enable input to E_L to emphasize that it is now active low. Memorize the definition of *active low* and *active high*. And then

a. Write out the Truth Table of the logic circuit with active high enable
b. Write out the Truth Table of the logic circuit with active low enable
c. Describe in words the difference in the circuit's operation when the enable is active high and when it's active low

7. In the last problem we introduced active high and active low enables. The objective of this problem is to introduce active high and active low inputs. Given the circuit of Problem (2) with everything active high as follows

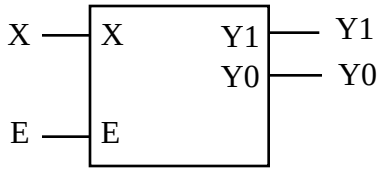


the corresponding circuit with an active low input is as follows

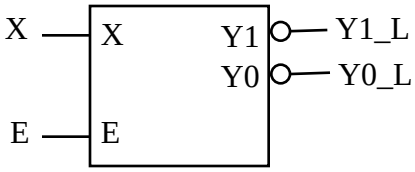


It operates the same as the circuit with active high input except that now the circuit's inputs are inverted before getting into the circuit. Write out the Truth Table for this logic circuit with active low input.

8. The objective of this problem is to introduce active high and active low outputs. Again starting with the circuit from Problem (2) with all inputs and outputs active high as follows



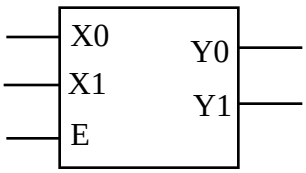
the corresponding circuit with active low output is as follows



It operates the same as the original circuit except that all the outputs are inverted before leaving the circuit. Write out the Truth Table for this logic circuit with active low outputs Y1_L and Y0_L

9. For the logic circuit of Problem (2)
   a. Draw the logic diagram when the input is active high, the enable active low and the output active low.
   b. Write out the Truth Table for your circuit in part (a)

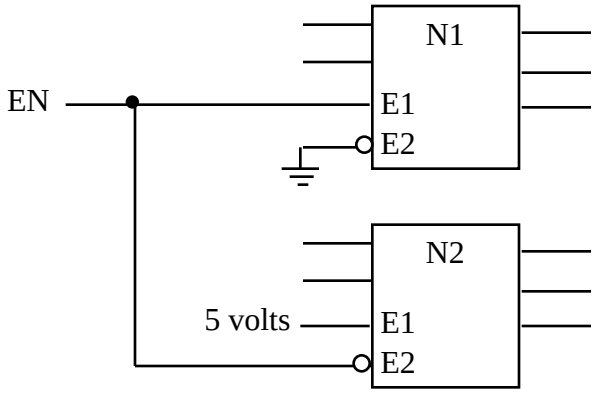
10. Given the following chip diagram and its truth table



E	**X1**	**X0**	**Y1**	**Y0**
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	0

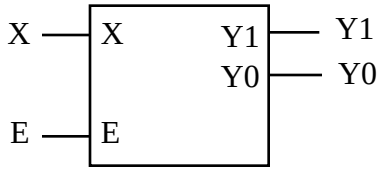
   a. Draw the chip diagram for the circuit when both the enable E and outputs Y1 and Y0 are active-low
   b. Write out the truth table for your circuit in part (a) with E_L, Y1_L and Y0_L

11. Given that the chips in the following circuit are enabled when E1·E2 is TRUE

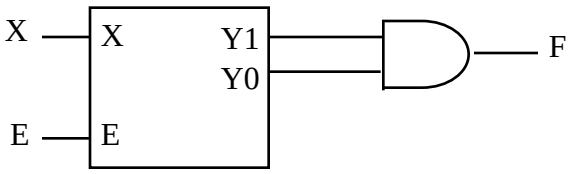


What is the value of EN when
a. N1 is enabled
b. N2 is enabled

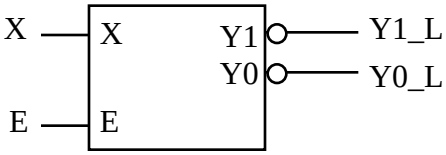
12. The real challenge in working with active low and active high signals is keeping track of everything when we connect logic circuits together. Let us begin with a circuit all of whose signals are active high as follows



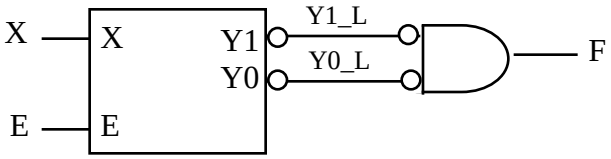
and for which we want to connect up a gate to obtain $F=Y1\cdot Y0$. This is easy. All we have to do is connect up an AND gate as follows



Now suppose that we again want $F=Y1\cdot Y0$ but now our circuit has active low outputs as follows

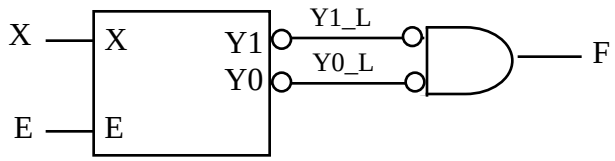


A good methodical way to accomplish this is to simply invert Y1_L and Y0_L and then pass the results through an AND gate as follows

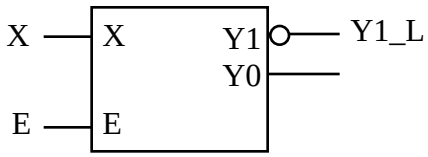


with inverting bubbles at the input of the AND. Now redraw the logic circuit with the AND gate and "bubble" INVERTERS replaced by an OR gate and an INVERTER. Explain how you got your result.

13. When we look at the logic circuit from Problem (9) as follows

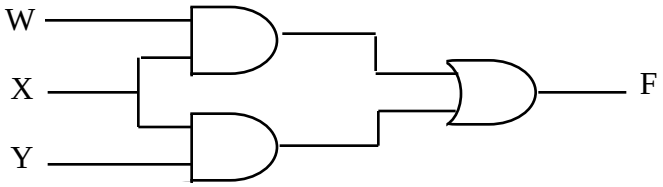


we see that the inverter bubbles come in pairs and so negate each other. Wakerly refers to this as "bubble-to-bubble" design. Make use of "bubble-to-bubble" design to obtain F=Y0+Y1 for the following circuit



with Y0 active low and Y1 active high. Make your final circuit for F from AND gates, OR gates and INVERTERS.

14. The objective of this problem is to introduce the term **levels of logic** - the maximum number of gates input signals must go through to reach the output.
    a. Explain why the following circuit has two levels of logic



    b. Draw a logic circuit with three levels of logic
    c. Why do we want the number of levels of a logic circuit to be as small as possible. Illustrate by drawing a graph showing the time delay between the input and output of a logic gate.