ECE 204L - COUNTERS - LAB 21
ANALYSIS OF SYNCHRONOUS COUNTERS

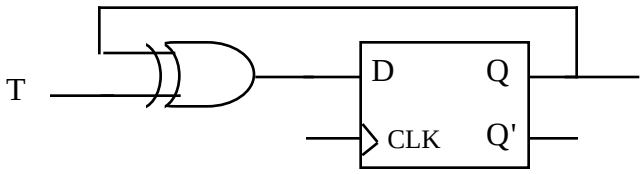
WINTER 2004 **A.P. FELZER**

OBJECTIVE

The objective of this lab is to build and test a synchronous counter.

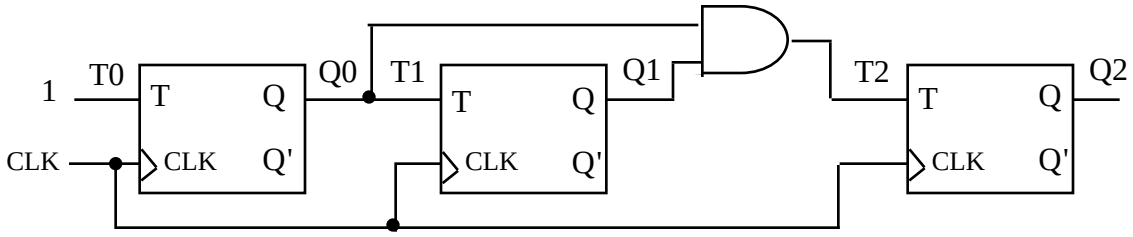
LAB

1. Verify that a general T flip-flop can be realized with a D flip-flop as follows



by showing that it has the same next state equation

2. Given the following 3-bit synchronous counter



a. Draw a logic diagram with pin numbers for this circuit with the T flip-flops implemented with D flip-flops
b. Calculate the counter's next state table.
c. Make use of your result in part (b) to draw the counter's state diagram
d. Build the circuit and then take measurements to obtain the circuit's next state table. Make use of preset and clear to start the counter at zero with $X_2X_1X_0 = 000$. Make use of your 7-segment display to display the results
e. Make use of your measurements in part (d) to draw the counter's state diagram
f. Compare your measured and calculated results
g. Make use of your measured results to obtain the circuit's timing diagram starting from the state Q2=Q1=Q0=0
h. Why do we call this counter a synchronous counter
i. What happens after 8 clock pulses
j. Is this an up-counter or a down-counter. How can you tell