ECE 204L - FLIP-FLOPS AND LATCHES - LAB 18
INTRODUCTION TO FLIP-FLOPS

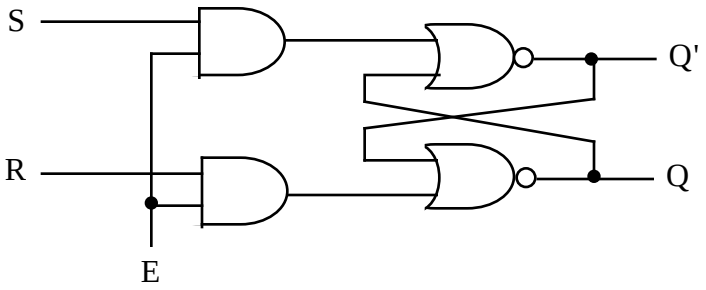
WINTER 2004 **A.P. FELZER**

OBJECTIVE

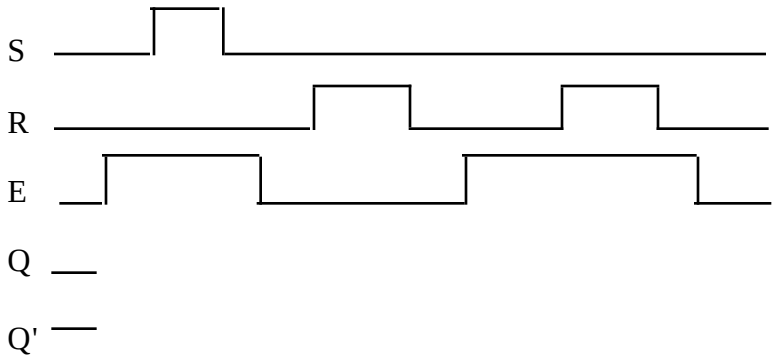
The objective of this lab is to build and test master-slave edge-triggered D flip-flops.

LAB

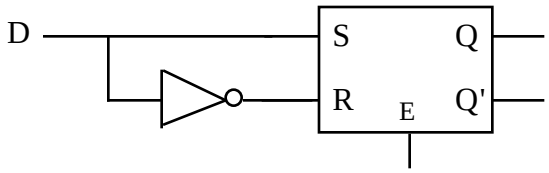
1. Given the following SR latch with enable signal E



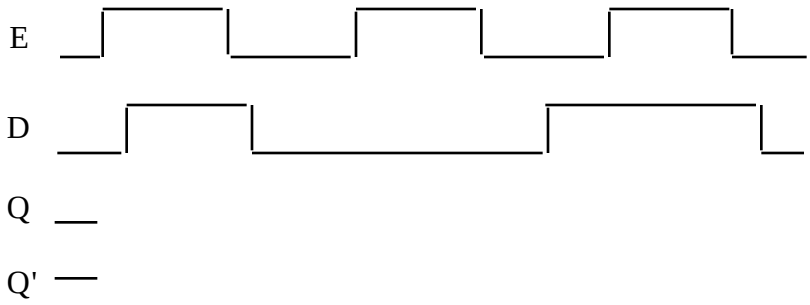
   a. Build and test your circuit. Carefully document your results. Use a DIP switch for S, R and E. As before be sure to put E on the left in your truth table
   b. Make use of your measured results in part (a) to complete the following timing diagram



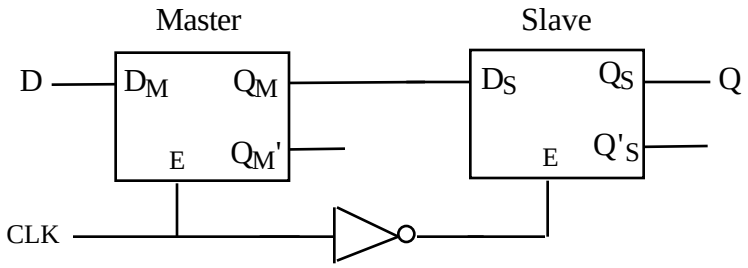
2. Given the following D latch made from the SR latch of Problem (1)



   a. Build and test your circuit. Carefully document your results. Use a DIP switch for D and E
   b. Make use of your measured results in part (a) to complete the following timing diagram



3. Given the following master-slave edge-triggered D flip-flop made from D latches of Problem (2) as follows



a. Build and test your circuit. Carefully document your results. Use LED's at D, Q_M and Q
b. Make use of your measured results in part (a) to complete the following timing diagram