ECE 204L - COMBINATIONAL BUILDING BLOCKS - LAB 14
MULTIPLEXERS AND TRI-STATE OUTPUTS

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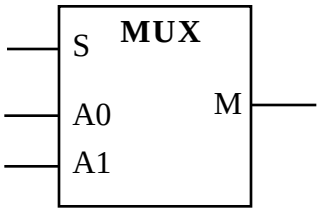
OBJECTIVE

The objective of this lab is to show how both multiplexers and tri-state outputs enable signals to share buses.

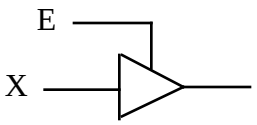
LAB

1. Given a 2-input, 1-bit MUX as follows



   a. **Prelab** - Explain in words what this MUX is doing
   b. **Prelab** - Write out the truth table for the MUX
   c. **Prelab** - Design the circuit with AOI gates
   d. Build and test your circuit

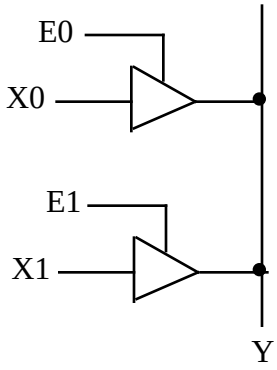
2. Given the following tri-state buffer



   a. **Prelab** - Write out the truth table for this tri-state buffer
   a. **Prelab** - Explain in words what this tri-state does

3. **Prelab** - Draw a chip diagram of a 74126 tri-state buffer

4. Given two tri-state buffers connected to a bus B as follows



   a. **Prelab** - Write out a truth table for the above circuit. Note that E0=E1=1 are not allowed because we want only one signal to be on the bus at any given time
   b. Test and document the operation of the circuit for each set of allowable inputs. Note that

the output B at any given time can be 1, 0 or open

c. Make use of your measured results to complete the following timing diagram